An Investigation on Speed Control of Permanent Magnet Synchronous Motor Drives Using FPGA: Conventional, Modern and Hybrid Control

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(FPGAを用いた永久磁石同期電動機駆動速度制御の開発：従来手法, 現代手法及び複合制御)

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A dissertation submitted in the partial fulfilment for the degree of

'Doctor of Philosophy' in Engineering

to

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2021

Acknowledgement

First and foremost, I would like to express my special gratitude to my supervisor Prof. Tsuyoshi Hanamoto, for granting me the freedom to pursue the research ideas that have been led to completion of this dissertation. Hanamoto sensei has inspired me with his polite and brilliant suggestions for research and life. I also like to thank Hanamoto sensei most sincerely for giving me the opportunity to work under his fruitful guidance. He has been supportive and contributed immensely for successful completion of this thesis.

I sincerely thank to professors of committee, Prof. Ichiro Omura, Prof. Masayuki Watanebe and Prof. Shyam S. Pandey for reading my thesis and giving me the enormous suggestions to make it more effective and concrete. I am thankful for their contribution and vast ideas to make my thesis more elaborative.

I shall extend my special thanks to my senior Ravikant Pandey, Ravi Nath Tripathi, Vijay Kumar Sing who has supported me during my study in japan and they had gone to their limits for helping and supporting me during good and bad times both.

I would like to thank Ikeura, Ohta, Ishibashi, Matsumono, Aonuma, Rajesh, Sagar. These guys with in the same lab made my three years of study very enjoyable and fruitful. I also like to thank all the member of Hanamoto laboratory for planning different parties, trips, game and supporting me during my stay and research in last three years..

I would like to thank my all Indian friends living in Kitakyusu Japan specially, Rudali, Mallikarjun, Anusha, Mehmuda, Ajendra,, and shubham for their wonderful company in here. I always felt like Kitakyushu is second home just because of you guys.

I would like to express my gratitude to Kyutech teaching and non-teaching staff, JASSO, Rotary Yoneyama Scholarship foundation, FAIS for supporting my study and stay in Japan. I would like to specially thank Japanese language teachers for their experienced teaching and effort to teach Japanese language.

I also like to thank and express my gratitude to my host family and the local people of Kitakyushu, Japan for their peaceful hospitality and I enjoyed playing, jogging, cycling, living in this beautiful country.

At last I would like to thank my parents for their blessing and encouragement for my study. I also like to thanks my brother for his time to time suggestions for maintaining my good health and interesting life throughout the academic career.

ABSTRACT

The permanent magnet synchronous motor (PMSM) has a key role to play in the motor drive system due its high efficiency, high torque to weight ratio, high power density, small size, less noise and lower rotor inertia. Moreover due to the lower maintenance cost and high reliability these motors has applications in low power range such as robotics, actuators and machine tools, as well as in high power range such as industrial drive, hybrid vehicle, and traction. Therefore depending upon the specific applications an appropriate controller is always requisite to achieve the desired accuracy in the motor performances.

The control strategy such as field oriented control (*FOC*) *has implemented for the industrial drive applications due to their simple structure and robustness. This control strategy utilizes cascaded proportional and integral* (*PI*) *controller for the outer speed controller and inner current controller loop, consequently it may leads to the sluggish behavior of motor drive system. The model predictive control* (*MPC*) *as an advance control method has acquired considerable attention for the control of the PMSM drive system. Amongst the various MPC the finite set model predictive control* (*FS-MPC*) *accounts discrete nature of the power converter with finite number of the switching states. A discrete motor model, a predictive model and a cost function for the selection of the optimized voltage vector for the power converter are the key steps required for the implementation of MPC control algorithm. By minimizing the cost function, the motor will reach the desired behavior defined by the function that compares the output of the predictive model with a reference. The Implementation of the MPC for the motor drive system increases the system complexity, therefore the real time implementation of the control is difficult to ensure in the sequential based digital signal processing* (*DSPs*).

Recently, due to the parallel processing nature and low power consumption the field programmable gate array (*FPGA*) *is an alternative for the implementation of the complex systems. However the FPGA based time-synchronization of control loop is a vital aspect concerning sampling time for discrete-time controller. The control loop of the motor drive system consisting of a speed controller and a current controller* (*PI based or MPC based*).

Time constant of the speed controller is different as to the current controller. In general, the sampling rate of the motor speed data is slower as compared to that of the sampling rate of the motor current data. As the control loops operates at different data sampling rate, the impact of time synchronization between these controllers is a crucial concern considering the transient conditions. In this work an FPGA based design and development of PMSM drive system considering the impact of time-synchronization for feedback control loop is considered.

The dynamic response of FS-MPC is one of the major factors that stands out amongst the controller family. Nevertheless, the motor speed regulation required additional control and generally a conventional PI controller is used. In this work, a two-degree-of-freedom (*2-DoF*) *control strategy is considered to enhance the dynamic performance of motor speed regulation. The 2-DoF control design is consisting of a conventional PI controller and an additional proportional gain as a feedforward loop. The 2-DoF control along with FS-MPC is employed for the PMSM drive system.*

The FS-MPC exploits the advantages such as high dynamic response and flexibility. However, the spread spectrum due to variable switching frequency of FS-MPC is the main drawback associated with it which leads to the filter and thermal designing more difficult. In this work, a predictive control strategy with fixed switching frequency is proposed. A discrete adaptive based hysteresis current control (*DAHCC*) *is combined with the basic FS-MPC as current controller to achieve constant switching frequency.*

The FPGA based implementation has disadvantage of the lacking the flexibility to change the system parameter. In this work, a python development environment on Xilinx Zynq device is considered for the online parameter optimization. Xilinx system generator (*XSG*) *as a digital simulator that is an integrated platform with MATLAB/Simulink is used for the designing and implementation of the controller algorithm.*

PUBLICATIONS

Journal Papers

(1) **I. Mishra**, R. N. Tripathi, and T. Hanamoto, “Time synchronization analysis of feedback control loop for FPGA-based PMSM drive system”, *Electronics*, vol. 11, no. 9, 1906, November 2020, doi: 10.3390/electronics9111906.

(2) **I. Mishra**, R. N. Tripathi, V. K. Singh and T. Hanamoto, “Step by Step Development and Implementation of FS-MPC for FPGA based PMSM Drive System”, . Electronics 2021, 10, 395. https://doi.org/10.3390/electronics10040395.

Conference Papers

(1) **I. Mishra**, R. N. Tripathi and T. Hanamoto, "Two-degree-of-freedom (2DOF) Speed Control based FS-MPC for PMSM Drives," *2020 23rd International Conference on Electrical Machines and Systems (ICEMS)*, Hamamatsu, Japan, 2020, pp. 1230-1234, doi: 10.23919/ICEMS50442.2020.9290973.

(2) **I. Mishra**, R. N. Tripathi, V. K. Singh and T. Hanamoto, “XSG based Comparative Analysis of FCS-MPC and FOC for PMSM Drive”, 3rd International Conference of Engineering Innovation (ICEI 2020) , Pattaya, Thailand, accepted.

(3) **I. Mishra**, R. N. Tripathi, V. Kumar Singh and T. Hanamoto, "Discrete Adaptive HCC Based FS-MPC with Constant Switching Frequency for PMSM Drives," 2019 22nd International Conference on Electrical Machines and Systems (ICEMS), Harbin, China, 2019, pp. 1-6, doi: 10.1109/ICEMS.2019.8922261.

(4) **I. Mishra**, R. N. Tripathi, V. K. Singh and T. Hanamoto, "A Hardware-in-the-Loop Simulation Approach for Analysis of Permanent Magnet Synchronous Motor Drive," 2019 10th International Conference on Power Electronics and ECCE Asia (ICPE 2019 - ECCE Asia), Busan, Korea (South), 2019, pp. 1-6.

(5) **I. Mishra**, R. N. Tripathi, V. K. Singh and T. Hanamoto, “Comparative analysis of continuous PWM and discontinuous PWM for PMSM drive,” 6thInternational Symposium on Applied Engineering and Sciences (SAES 2018), Japan, presented.

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

Chapter 1

INTRODUCTION

In the last few decades, the use of power converters and high-performance adjustable speed drives has gained an increased presence in a wide range of applications, mainly due to improved performance and higher efficiency, which lead to increased production rates. In this way, power converters and drives have become an enabling technology in most industrial sectors, with many applications in a wide variety of systems. Conversion and control of electrical energy using power electronics is a very important topic today, considering the increasing energy demands and new requirements in terms of power quality and efficiency. In order to fulfill these demands new semiconductor devices, topologies, and control schemes are being developed.

1.1 Applications of Motor Drives

The power/energy conversion is the essential part of an electrical power system. The electrical motors are one of the major parts of electromechanical energy conversion (EMEC) system that is used for conversion of electrical energy into mechanical energy. The motors have been used in a wide variety of applications such as domestic appliances, industry, fans, and pumps are those that account for most of the energy consumption, with power ratings up to several megawatts [1], [2], [3], [4]. Depending upon the specific applications, specific motors need to be chosen. Fig.1.1 shows the main types of motors. The motors can be broadly classified in to direct current (DC) motors and alternating current (AC) motors. Further these are classified depending upon the principle of conversion (electromagnetic motor, electro static motor, and ultra-sonic motor), power supply (DC power supply, single phase AC power supply, three phase AC power supply). The main categories of the motors is listed in the Table 1.1 with their basic characteristics.

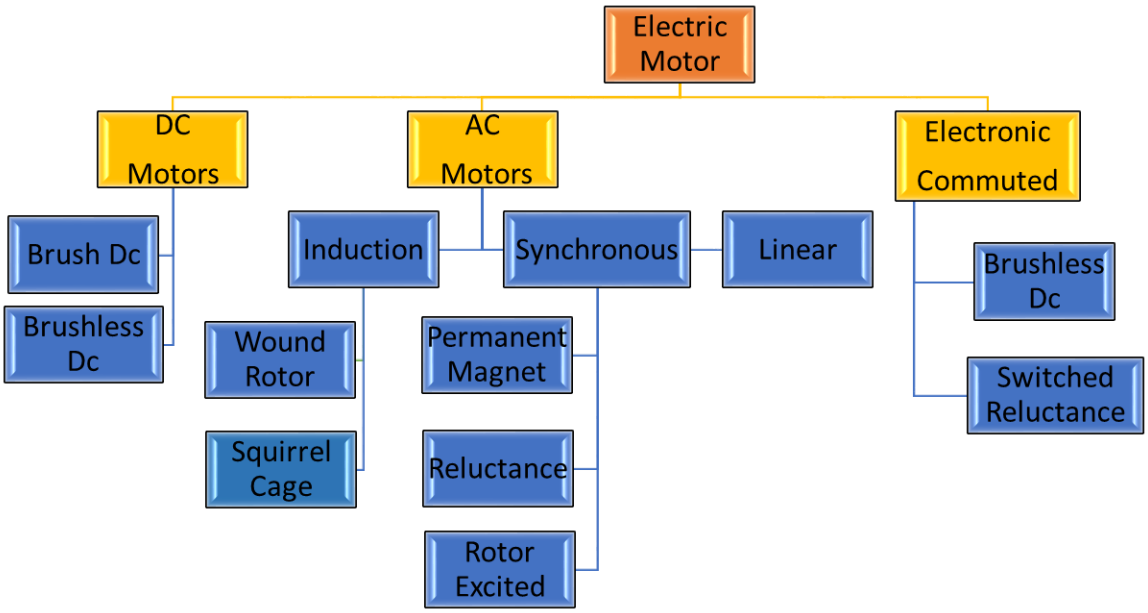


Fig.1.1 Types of Motors

Table 1.1 Motor Chareteistics

	Induction motor	Sync motor	Brushless DC motor	Servo Motor	Stepper Motor
Efficiency	60-70%	70-80%	80%	50-80%	55-65%
Response	Slow	Slow	Medium	Fast	Slow
Speed range	Wide	Wide	Wide	Medium	Wide
Size	Large	Medium	Small	Small or Medium	Small

The motor performance and efficiency can be improve by the use of adjustable speed drives. Many interesting applications of high-power drives can be found in the fans, blowers, pumps, machine tools, power tools, turbines, compressors, alternators, ships, rolling mills, paper mills, movers, mining industry, in downhill belt conveyors and other special applications.. Common applications of drives can be found in transportation [5], [6], where electric motors are used for traction and propulsion. In electric trains, the power is transferred from the overhead lines to the motors using a power converter. This

converter generates the required voltages for controlling the torque and speed of the electric motor used in the trains. High-power drives can be found in ships [7], [8], where diesel engines are used as generators and the propulsion is generated by electric motors.

Now a days, the motor drive applications can be found in electric and hybrid vehicles, and in aircraft. In hybrid electric vehicle (HEV), different motors works at different speeds. The battery use for the electric motor need a battery which is charged by the regenerative braking and internal combustion engine. The battery can also power auxiliary loads and reduce engine idling when stopped. Together, these features result in better fuel economy without sacrificing performance [9], [10]. Aircraft applications demand high reliability, high availability, and high power density while aiming to reduce weight, complexity, fuel consumption, operational costs, and environmental impact. New electric driven systems can meet these requirements and also provide significant technical and economic improvements over conventional mechanical, hydraulic, or pneumatic systems. Therefore advance power electronics based drive system can play a crucial role for the modern days applications.

Besides these high power applications the motor drives system has also applications in the domestic appliance such as microwave, washing machine, refrigerator, hair dryer, electric fan, smart phones, vacuum cleaner air conditioner etc... The use of the adjustable speed drives can improve the efficiency of the motors for these residential applications. The motor drives has also applications in miniature vibration motor pumps of power rating 0.2 W. However, in recent years, demand for more compact, reliable and energy efficient products has increased.

Nowadays a lot of attention is dedicated to an improvement of variable speed ac electric drives in order to satisfy increasing demands in quality and reliability. Extremely fast development on the field of power-electronics over the last few decades enabled a use of advanced switches and power inverter topologies, which yield lower total harmonic distortion (THD), higher efficiency, higher reliability, lower costs and significantly improves the overall drive behavior. The need for more accurate control requires to

consider not only the drive itself but also its supply (with LC or LCL filters) and load (e.g. with pump, linear motion and weight lift). The complexity of the control algorithms is thus significantly increasing. Both the motor designing along with its controller developments plays a key role in motor drive systems. Therefore, development of a control algorithms can be challenging task to achieve the desirable response with high efficiency depending upon its applications.

1.2 Control of Power Converters motor Drives

Power converters are consists of power semiconductor devices and passive components. These can be classified depending upon type of conversion from input to output of the system (AC and DC) is listed in the Table 1.2. Under these categories they may have the sub categories. Depending upon the applications different power converters can be used for the controller implementation.

Table 1.2. Converter classifications.

Converter	Working Principle
AC–DC	Conversion from AC to regulated or unregulated DC voltage or current.
DC–DC	Conversion from a DC input voltage to a DC output voltage, providing regulation of the output voltage and isolation.
DC–AC	Conversion from a DC voltage or current to an AC voltage or current with controlled (variable) amplitude, frequency, and phase.
AC–AC	Conversion from an AC voltage with fixed magnitude and frequency to an AC voltage with controlled (variable) amplitude and frequency.

Several control methods have been proposed for the control of inverters and drives, the most commonly used ones being shown in Fig. 1.2. Some of these are very well established and simple, such as the nonlinear hysteresis control, while newer control methods, which allow an improved behavior of the system, are generally more complex or need much more calculation power from the control platform. Hysteresis control takes advantage of the nonlinear nature of the power converters and the switching states of the power semiconductors are determined by comparison of the measured variable to its

reference, considering a given hysteresis width for the error. This is the simplest controller with an advantage of low computation.

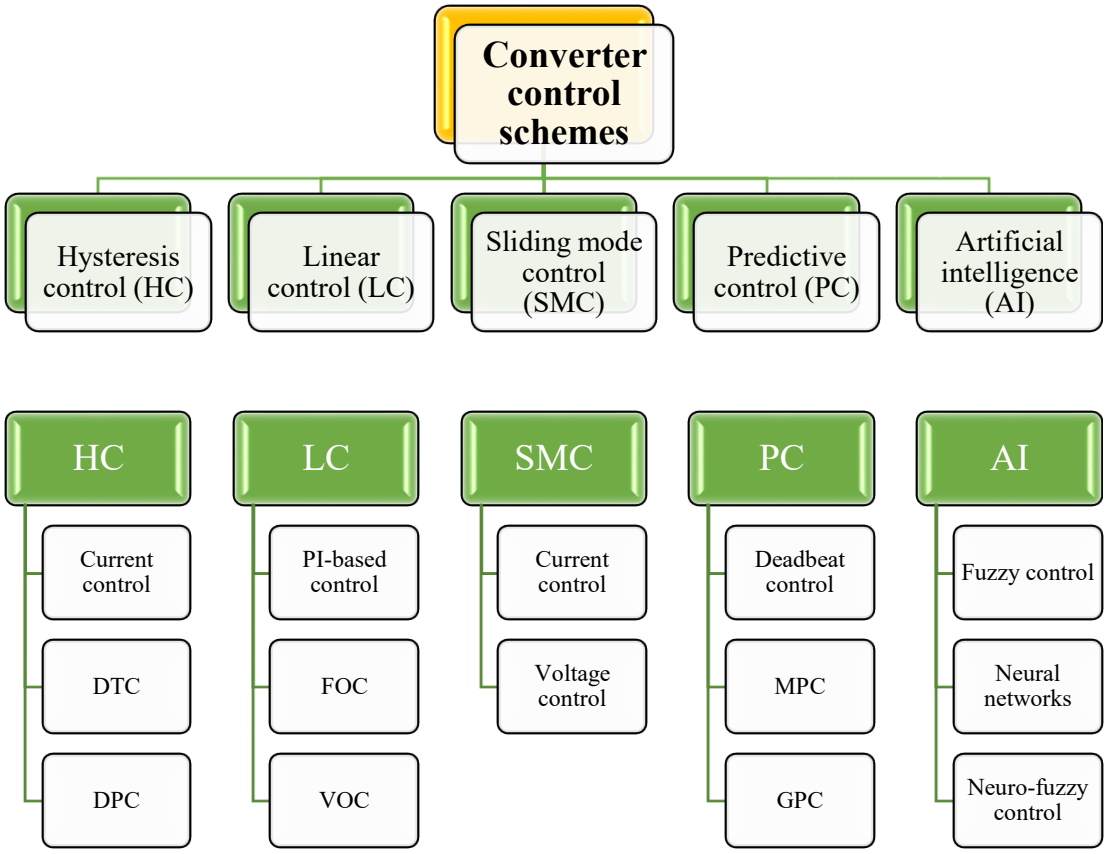


Fig.1.2. Different types of converter control schemes for power converters and drives.

This controller has the application as a current controller in the grid connected applications [11], [12]. Moreover this controller is also implemented as a current controller for the motor drive system [13],[14]. However, these controller also has used for more complex schemes such as direct torque control (DTC) [15], [16] and direct power control (DPC) [17], [18]. This control algorithm has been implemented in analog electronics. However, for the implementation in a digital platform, a very high sampling frequency is required. The main drawback with the hysteresis controller algorithm is: the width and the nonlinearity of the system inherently introduce variable switching frequency. This may lead to wide range of spectrum and also may create resonance problems in some

applications. The filter design with this spread spectrum is a very difficult task. In literature many new idea have been implemented to achieve constant switching frequency.

Another category of the controller algorithm is the linear based controller. This linear controller have a modulation stage such as sinusoidal pulse width modulation (SPWM), space vector modulation (SVM), third harmonic elimination modulation (SHEPWM) and bus clamping PWM etc. for the generation of the switching signals for the power converter. The most commonly used in the industrial applications is the proportional–integral (PI) controllers. The PI controller based controller algorithm is implemented for grid connected converter as voltage oriented control (VOC) [19], [20]. A well-known control method for drives, based on linear controllers, is field oriented control (FOC) [21]. The linear control scheme with a modulation stage often requires additional coordinate transformations. In addition, the fact that a linear control is applied to a nonlinear system can lead to uneven performance throughout the dynamic range. Moreover, today's digital implementation requires sampled data control schemes that are an approximation of the continuous-time linear controller. All this, together with the additional modulation stage, introduces several design steps and considerations for achieving a suitable control scheme, which can be very challenging for some power converters such as matrix, multilevel converters, etc. Furthermore, power converter systems are subject to several system constraints and technical requirements such as total harmonic distortion (THD), maximum current, maximum switching frequency, etc. which cannot be directly incorporated into linear controller design. In summary, classical control theory has been adapted over and over in order to use it in modern digitally controlled converters. With the development of more powerful microprocessors, new control schemes have been proposed.

Sliding mode control is a nonlinear control, which algorithm implementation is based on variable structure control strategy. This is an effective and high frequency switching control for nonlinear systems with uncertainties. The sliding mode current control is fist propose for motor drive system in 1977 for the disturbance rejection, robustness implementation. The sliding mode current control for FOC for motor drive

system has been used for industrial applications. [22], [23]. The sliding mode voltage control and current control has also implemented for grid connected systems [24], [25]. This controller has its advantages such as it has symmetric designing procedure, robust control scheme against matched external disturbances and unpredictable parameter variations. However, this controller algorithm has some disadvantages that may cause huge damage in the system that is: chattering problem. Some modifications has been applied to the classic SMC in order to overcome this problem and improve its performance [26].

Recently artificial intelligence based control such as neural network and fuzzy control has been implemented in many applications in motor drives [27], [28]. The fuzzy control has many advantages such as they are more readily customizable in natural language terms, they cover a wider range of operating conditions, and they are cheaper to develop. In neural networks have the ability to learn by themselves and produced the output that is not limited to the input provided to them. The input is stored in its own networks instead of the database. Hence, data loss does not change the way it operates. The neural network performs multiple tasks without affecting system performance. Moreover, if any information is missing, the network can detect the fault and still produce the output. Despite of all these advantages these controller has their own disadvantages such as they are completely dependent on human knowledge and expertise, regular updating of the rules of a Fuzzy Logic control system.

Predictive control has been receiving popularity for the control of power converters and drives [29]–[30]. It comprises a wide family of controllers with different approaches. Predictive control is characterized by the use of a model of the system to predict the future behavior of the controlled variables, and the use of an optimization criterion for selecting the optimum actuation. The deadbeat control, one of the basic predictive control, uses the idea where a prediction is made for the optimum actuation so that the error between the reference and the controlled variables will be zero at the next sampling instant for the first-order system. Among the various classifications of predictive control, model predictive control (MPC) is one of the most popular control schemes due to its several attractive

features. MPC is the main focus of this thesis and the detailed explanation with the literature review is presented in the next subsection.

1.3 Research Background

Permanent magnet synchronous machine (PMSM) has become the most promising drive motor candidate for low power range applications such as robotics, actuators, and machine tools [31], [32], [33] as well as in high power applications for industrial drives, vehicular propulsions and traction [34], [35], [36] due to its high power density, high torque to weight ratio, and higher efficiency and low maintenance cost. Compared with induction motor, PMSM does not need magnetizing component of stator current, since the excitation is provided by permanent magnets inside the machine. This increases the efficiency and also reduces the overall system cost. Besides, PMSM can be designed with less weight and volume over the induction machines. They also have higher torque to the inertia ratio which is very important for the fast electrical and mechanical dynamic responses.

In order to drive the PM machine with high efficiency and stability, different control methods for PMSMs have been developed corresponding to the system applications to achieve desired motor speed and smooth transition considering change in motor load conditions. In general, there are two basic control strategies for PMSM: open-loop control and closed-loop control. In the open-loop control (V/f control) methods [37], the motor variables (such as the stator voltage and current, the rotor position and speed) need not to be feedback for the controller development. The voltage and frequency commands will be given by the controller without the comparison with the actual values. Due to this the open loop control implementation is easier. However, in the high performance drive systems, good stability and robustness can be achieved by closed-loop control method (such as vector control and direct torque control). For the closed loop control implementation the motor speed current, rotor position and speed need to be feedback.

Several linear and nonlinear control has studied and implemented for PMSM close loop control. The nonlinear control such as hysteresis control is studied for the motor drive system [38]. In this control the reference value is compared to the measured value, the error

obtained from this is passed through a fixed band for the generation of the switching pulses for the power devices. This controller has its own advantage such as simple structure, however, they have a better performance at higher sampling time and also have variable switching frequency. To overcome this issues an adaptive based hysteresis current control has been proposed. In the linear control such as the PI based FOC PMSM drive has been implemented for industrial applications because of its simple structure and reliability [39-40]. The control implementation uses the rotor speed as feedback for generating the reference torque and uses the rotor position for decoupling the stator currents, and then the torque component of the current can be controlled precisely. In FOC, the flux and torque of AC machines can be separately controlled as DC motors [41]. Over the years, FOC drives have achieved a high degree of maturity in a wide range of applications. They have established a substantial worldwide market which continues to increase [42].

The control algorithm for motor drive system has been developed using digital signal processors (DSPs) [43-45]. However, the DSP based implementation suffer from long execution time and high memory allocation of the CPU. Considering the above demerits of the DSP, the field programmable gate array (FPGA) having advantages of parallel processing, programmable hard-wired feature, fast computation ability, shorter design cycle, and embedded processor, is more effective for the controller execution [46-48]. In [49], an FPGA based FOC for PMSM drive is developed and FPGA based architecture for the sensor less speed control of PMSM is presented in [50].

The feedback control loop of the motor drive system consisting of a speed controller (outer control loop) and a current controller (inner control loop). The time constant of the speed controller loop is different as to the current control loop [51]. The performance of the motor drive system is governed by the bandwidth of the current control and switching frequency selection is crucial to achieve the desired bandwidth [52, 53]. However, the increase in switching frequency will ultimately lead to the higher system losses.

Besides the switching frequency, the digital implementation of control involves the vital role of sampling frequency for the performance of motor drive system [54]. Nevertheless, the sampling frequency is having vital impact on system performance

especially during transient condition. There is no specific criteria available to decide the appropriate selection of sampling frequency. In [54], a lower limit is mentioned corresponding to a specific control and the bandwidth can be taken as one by sixth of the sampling frequency. Furthermore, the digital delay of the control loop that is consisting of throughput time of AD converter, delay introduced by converter in terms of dead time, computation time for control execution constrained the controller bandwidth [52]. Consequently, the role of sampling frequency involves more complexity considering the performance of motor drive system.

In general, the sampling rate of the speed controller is slower as compared to that of the sampling rate of the current controller. As the control loops operate at different data sampling rate, the impact of time synchronization between these controllers is a crucial concern considering the transient conditions corresponding to the sampling rates. The motor speed is related to mechanical parameter and the sampling rate is predefined corresponding to the encoder setting. The sampling rate of the motor current is possible to control corresponding to the maximum possible throughput rate of AD converter. Consequently, the performance of current control loop can be influenced under transient condition.

In case of motor drive system, the impact of sampling frequencies (throughput rates) is not yet analyzed categorically. The impact of sampling frequencies is required to probe the performance of the controller under transient conditions because the higher throughput rate not necessarily will result in improved performance. In addition, the indirect impact of throughput rate on speed controller is also one of the key point corresponding to a change in reference speed of the motor. The repercussion of time synchronization on control loops corresponding to sampling frequencies is another crucial concern considering the transient conditions: change in reference speed and load disturbance.

Another controller the DTC has been implemented for the motor drive system for different applications. Different from FOC, DTC firstly observes the stator flux by flux observer, then determines the sector where the stator flux is located. Next, it calculates the

electromagnetic torque, then the actual flux and torque will be compared with the reference, and a bang-bang control is usually adopted. Combing with the stator flux sector signal, appropriate voltage space vector is selected to control the stator flux amplitude to be constant and the change of the torque angle to achieve a direct torque control of the PMSMs. DTC has low dependence on motor parameters. Stator resistance is the only parameter used when observing the flux linkage. The system has high robustness. Directly taking the motor torque as the control object eliminates the current control link and has good dynamic performance, even the torque dynamic response of a DTC drive system can be ten times faster than any other AC drive [55].

In the case of the conventional control, the system complexity increases with the inclusion of the control parameters. The DTC have a good dynamic performance however, it has poor steady state performance. The implementation of FOC, one outer speed controller and two inner current controller need to tune separately. With change of working conditions, the drive performances may worsen [56].The inner current control loop, have a crucial role in motor drive system to generate the reference voltage, which ultimately generates switching signal. For the small and medium power motor drive system the current loop bandwidth is restricted due to the limited switching frequency, which directly impact the system dynamic performances [57]. Moreover, the motor current is regulated by the terminal voltage applied by an inverter, above medium speed range if abrupt reference change is applied, the reference voltage generated from the current control loop may undergo saturation. Finally its leads to the degradation in the current regulation [58]. To achieve fast dynamic response with and better current regulation a better controller is always desirable.

The model predictive control (MPC) is an advance control strategy that can improve the dynamic response by predicting the next step current [59]. Moreover the MPC possesses attractive features such as direct use of the system model and simultaneous multiple constraints handling nature to deal with multiple control parameters [60], [61], [62]. By considering these appealing characteristics, MPC is gaining attentions among researches, and also have been applied to wide variety of drive applications. A generalized

predictive control is proposed and analyzed in [63] for PMSM drive system. In [64], a multi-variable predictive control is achieved for PMSM based on states equation. A digital predictive current controller with delay compensation is adopted in [65], to achieve high bandwidth discrete time current controller for voltage source pulse width modulation (VS-PWM). Moreover, to ensure a perfect tracking the author consider an adaptive model for the estimated uncertainty dynamics. To achieve high speed control dynamics a model predictive direct speed control is implemented in [66], for PMSM drive system. In [67], a matrix converter fed predictive torque control is proposed for PMSM drive system.

The MPC implementation methodology utilizes the mathematical model of the plant to predict the future behavior and further an optimization function is used for the selection of the switching signal. Among the various MPC algorithms the finite set MPC (FS-MPC) consider the finite set of the possible switching state of the power converter for the generation of the switching signal for the power devices [68],[69]. Compared with the general MPC the major advantage of FS-MPC is that it can directly generate the switching signal by optimizing the control parameter without any modulation stage. However, the cost function optimization problem is computed by a predicting all the possible switching states of the power converter in every sampling period. With the increase of the complexity in the converter system the system may undergo delay which ultimately degrade the system performance [70], [71].

The field programmable gate array (FPGA) having advantage of parallel processing nature which shortens the computational time, that ultimately leads to lower in the control delay and better system performance [72], [73]. Moreover, FPGA is considered as the better option for controller designing and prototyping due to its fast computation ability, embedded processor and shorter design cycle [74], [75]. In [76] an implementation methodology using the hardware description language (HDL) Coder from Math Works is presented with an automated workflow for implementing a long horizon FS-MPC for a PMSM drive system. At present, model-based design (MBD) for FPGA implementation of complex control systems becomes attractive because of the time-saving and great flexibility in simulation and debugging [77], [78], [79].

Despite several attractive features, the FS-MPC encounters some major drawbacks. The main drawback with this technique is variable switching frequency which ultimately leads to increase in switching losses, spread switching frequency spectrum and poor system performances. The switching harmonic spectrum depends on the commutations of the converter's power switches, which in FS-MPC is not guaranteed to occur at the fixed sampling frequency. Due to the variable switching frequency the filter design and the thermal design became more difficult which leads to the increase of the overall cost of the system.

To make the switching frequency constant many attempts were made in the past for different applications such as in grid connected system, motor drive system and multilevel inverter with RL load. The predictive control with discrete space vector modulation (DSVM) in [80] was implemented for the power converter. The main advantage with this approach is it gives good performance at the low sampling frequency, while the computational burden increases to achieve the objectives. A modified DSVM with FS-MPC [81] is proposed for the RL load to achieve constant switching frequency. In this paper, the author is able to reduce the common mode voltage with this technique, while the number of calculations increases. In [82] a modulated model predictive control was proposed for both the RL load and PMSM in the over modulation region. This method gives a fast dynamic response compared to the basic FS-MPC. However, the setting of the current at the reference signal gives a dip in the amplitude. The basic FS-MPC combined with a PWM modulator in [83] was implemented for the PMSM drive. In order to make the switching frequency constant, the voltage vectors are dynamically selected and calculated by an optimization algorithm. However, this method involves a large number of calculations for the evaluation of the suitable voltage vector which leads to an increase in the system complexity and computational burden.

Besides this issue the FS-MPC has nonzero steady-state error (SSE). This error is more significant when operated with lower switching frequency or lower amplitude of current reference. Several ideas has been proposed to overcome this issue, such as inclusion of constraints, and cascaded model predictive control. In cascaded model predictive control

the outer PI based speed controller is replaced by the model based speed controller. No doubt, the controller implementation increases the computational burden and also the system reliability decreases.

Furthermore, the speed regulation of motor system is imperative in the motor drive control. During the operation, the motor may undergo different kind of disturbance due to the change in load condition as well as change in reference speed depending on operating conditions. Due to the simple design and implementation, the conventional PI control is widely use to realize the speed regulation of the motor [84], [85].

The speed regulation in conjunction with inner current control loop governs the performance of the motor drive system. In the inner current control loop the FS-MPC is employed to improve the dynamic performance corresponding to change in operating condition of the motor drive system. However, the controller for speed regulation under achieve the performance due to limitation of conventional PI control that will ultimately impact the overall dynamic performance of the system.

The requirements to improve the dynamic performance under transient condition occurred due to an alteration in operating condition, is to reduce the settling time. Moreover, reduction in settling time can results in higher overshoot/undershoot during the transients. The fast dynamic response corresponding to the reference speed and a robustness to the load disturbance is always desirable through the speed controller design. Therefore, to obtain a better trade-off and optimized performance a sub-control is necessary that can be realized by incorporating additional controller gain along with conventional controller. This is defined as the degree of freedom of the controller.

The two-degree-freedom (2-DoF) PI controller was used for the PMSM control [86], [87]. There are various control design methods that are used for the speed control of the PMSM considering the degree of freedom of controller. The 2-DoF control for both the speed control and field-oriented inner current control of PMSM drive is analyzed in [88].

1.4 Research Objective

The various conventional, as well as modern control schemes, have been used in motor drive system, for the specific control objectives as discussed in the previous subsections. The control schemes have to deal with various pros and cons, however, every control scheme has its distinctive characteristics that make the particular control scheme more suitable for a specific application. The MPC, as a modern control scheme, is used in this study to control the PMSM. The objectives that are taken into account and the key contribution of the research are as follows:

The first procedure is to implement the conventional control (FOC) PMSM drive system and to search for the issues related to the control. The FOC based control for the motor drive system is commonly used in the industrial applications. The first objective is to map the control algorithm on to a digital simulator considering an FPGA-based implementation. In order to get a hassle-free HDL code required for FPGA to perform the real-time implementation, there is a need to develop the controller on to a digital simulator having the functionality of an automatic HDL code generation from the developed controller. Xilinx system generator (XSG), as a digital simulator of Xilinx, is used in this work for the design and development of the controller. However, the motor drive system development and prototyping is a tedious task considering a FPGA based real-time system implementation. In addition, the time-synchronization of feedback control loop is another vital aspect concerning sampling time for discrete-time controller. This work presents an FPGA based design and development of PMSM drive system considering the impact of time-synchronization for feedback control loop corresponding to sampling frequencies. A step by step and case by case time synchronizations methodology is considered to analyse the repercussion of sampling frequencies corresponding to feedback control loop synchronization. Moreover, the FPGA based implementation has disadvantage of the lacking the flexibility to change the system parameter. In this work, a python development environment on Xilinx Zynq device is considered for the online parameter optimization.

The control implementation needs to tune at least four parameters separately and with change of working conditions, the drive performances may worsen. The inner current control loop, have a crucial role in motor drive system to generate the reference voltage, which ultimately generates switching signal. For the small and medium power motor drive system the current loop bandwidth is restricted due to the limited switching frequency, which directly impact the system dynamic performances. Moreover, the motor current is regulated by the terminal voltage applied by an inverter, above medium speed range if abrupt reference change is applied, the reference voltage generated from the current control loop may undergo saturation. Finally its leads to the degradation in the current regulation. To achieve fast dynamic response with better current regulation a better controller is always desirable. The FS-MPC is an advance control strategy that can improve the dynamic response by predicting the next step current. In order to implement the control algorithm, the first procedure is to review various literature related to the MPC control applied to different power converters and to search for the issues related to the control. After that, to understand the algorithm of FS-MPC for the motor drive system. As the real-time implementation of FS-MPC is performed on digital platforms, the first objective is to map the control algorithm on to a digital simulator considering an FPGA-based implementation, an alternative way to handle the computational burden of the control algorithm.

The FS-MPC exploits the advantages such as high flexibility, and easy inclusion of constraints. However, the spread spectrum due to variable switching frequency of FS-MPC is the main drawback associated with it. The FS-MPC as a current controller generates the switching signal based upon the selection of the voltage vector corresponding to the optimized current error. Similarly, HCC generates the switching signal based on the current error passed through the hysteresis band. For both the cases, the main concern is the variable switching frequency. To overcome this drawback in HCC, it is combined with the modulation techniques, like that of the FS-MPC case. Moreover, an adaptive hysteresis band method is also used with conventional HCC to make the switching frequency constant. The optimized minimum error obtained from the FS-MPC can be used to generate

switching signals by passing through the discrete adaptive band HCC (DAHCC) that ultimately allow the controller to work at constant switching frequency.

The dynamic response of FS-MPC is one of the major factors that stands out amongst the controller family. The requirements to improve the dynamic performance under transient condition occurred due to an alteration in operating condition, is to reduce the settling time. Moreover, reduction in settling time can results in higher overshoot/undershoot during the transients. The fast dynamic response corresponding to the reference speed and a robustness to the load disturbance is always desirable through the speed controller design. Generally a conventional PI controller is used for speed controller. To obtain a better trade-off and optimized performance a sub-control is necessary that can be realized by incorporating additional controller gain along with conventional controller. This work presents a two-degree-of-freedom (2-DoF) control strategy to enhance the dynamic performance of motor speed regulation. The 2-DoF control design is consisting of a conventional PI controller and an additional proportional gain as a feedforward loop.

1.5 Outline of the Dissertation

In order to present the work, the dissertation is organized in the following manner. The dissertation is divided in to 6 parts including the introduction which are explained bellow.

Chapter 1: Introduction

This chapter presents an overview of motor drive applications in different sectors, role of power electronics converter circuits in the motor drive applications, the different control schemes used for the motor drives to handle the various control objectives. Moreover, a detailed literature background of conventional control such as FOC and DTC, the draw backs of these controllers and (FS-MPC) with the fundamental concepts and drawbacks associated with it is presented. Finally the objectives of the dissertation is presented along with the outline of the dissertation.

Chapter 2: FPGA-Based Development Platform and HIL Simulation

This chapter presents, different simulation methodologies that can be adopted for the system implantations. The DSP based implementation of the motor drive system and the drawback related to this approach is discussed. The digital implementation of the controller through the XSG based digital simulation environment, HIL simulations for the control pre-validation, and FPGA based implementation for the validation of the controller. Finally the advantages of the FPGA implementations for the motor drive systems.

Chapter 3: Conventional PMSM Drive: Field Oriented Control

This chapter presents an FPGA based design and development of PMSM drive system considering the impact of time-synchronization for feedback control loop corresponding to sampling frequencies. A step by step and case by case time synchronizations methodology is considered to analyse the repercussion of sampling frequencies corresponding to feedback control loop synchronization. The harmonics in motor current is also taken into account for different switching frequencies and sampling frequencies correspondingly. Furthermore, a step change in reference speed as well as load disturbance is introduced to investigate the transient/dynamic behaviour of the system. The controller is developed in the Xilinx system generator (XSG) environment integrated with the MATLAB/Simulink for the FPGA-based experimental system implementation.

Chapter 4: Modern PMSM Drive: Finite Set Model Predictive Control

This chapter, presents FPGA based real time implementation of FS-MPC for PMSM drive system. The FS-MPC algorithm is developed for a three phase two level voltage source inverter (VSI) fed PMSM drive system using an optimization function in terms of current. Step by Step design and development of the controller for the motor drive system is explained. The motor dynamics response is analysed corresponding to different sampling frequency. Moreover, the harmonics in the motor current is also consider corresponding to different sampling frequencies. To analyse the dynamic behaviour of the motor, a step change in the speed reference and load disturbance is introduced. Furthermore, a model based approach has been adopted for the system implementation for the modelling of the FS-MPC. For the real time implementation on FPGA, the controller is developed in XSG environment.

Chapter 5: Advance PMSM Drive, Hybrid Control: 2DOF-FSMPCand DAHCC-FSMPC

In this Chapter a 2-DoF PI controller is designed for speed regulation of PMSM along with FS-MPC. The 2 DoF controller design is consisting of two proportional gains and an integral gain. The dynamic response of the 2 DoF speed control is compared to that of the conventional PI controller for the load disturbance. The gain uses for the controller designing is obtained by the trial and error method. In addition to this, an adaptive HCC based FS-MPC for the VSI fed PMSM drive system which allows the system to work at predefined switching frequency. FS-MPC have inherently discrete nature and discrete adaptive HCC is designed for system implementation. In order to validate the system performance it compared with the FS-MPC. Moreover a model based approach has been adopted for the system implementation as in chapter 4 for modeling of FS-MPC. The simulation of the system has been done using the XSG and MATLAB/Simulink simulation environment for the HIL simulation.

Chapter 6: Conclusions and future work

The main conclusions of the dissertation and recommendations for future work are highlighted in this chapter.

Chapter 2

FPGA-BASED DEVELOPMENT PLATFORM AND HIL SIMULATION

2.1. Introduction

Control strategies for power converters and drives have been the subject of ongoing research for several decades in power electronics. Classical linear controllers combined with modulation schemes and nonlinear controllers based on hysteresis bounds have become the most used schemes in industrial applications. Many of these concepts go back to research on analog hardware, which limited complexity. Modern digital control platforms like DSPs have become state of the art and have been widely accepted as industrial standards. The main digital control platforms used in industrial electronics are based on fixed-point processor, due to the high computational power and low cost. However, in the academic world, control platforms based on floating-point processor with high programming flexibility are more usually used. Recently, hardware and software solutions implemented in field programmable gate arrays (FPGAs) have received particular attention, mainly because of their ability to allow designers to build efficient and dedicated hardware architectures by means of flexible software.

This part makes a comparative evaluation of the hardware programmable versus the software programmable computers for the control system of electrical drives.

2.2. Digital Signal Processing

A DSP is a complete computer that provides most required hardware peripherals embedded on a single chip. Integrating many peripherals such as memory blocks, memory controllers and etc., would lead to reduction of the system cost and improvement of the

computational performance. Further distinction of DSPs is the higher number of the basic instructions which the processor is capable to perform.

A big area of applications for DSPs is control of electrical drives. The main requirement for these applications is real-time operation. It demands performing all computations within a predefined discrete time. The strategy for meeting this requirement, in a cost effective way, is reducing the computational load of the CPU and assigning many of the tasks to the peripherals. It is customized for motor drive control applications. What is noticeable about it, is its floating-point unit making it powerful for complex mathematical calculations.

2.3. Field Programmable Gate Array

By increasing the density of logic elements of FPGAs, effective use of available resources becomes more and more challenging. The programming language and development environment have significant impacts on the effective usage of logic area on the one hand and shortening the design time on the other. To respond to the need for rapid prototyping of new FPGA-based systems, constantly new tools for programming and verification of FPGA configuration are introduced. Hardware Description Languages (HDL) are industry standard tools for describing models to be implemented on FPGAs.

However, writing specific HDL codes needs special training and hence, it is considered a complex and time-consuming task even for skilled researchers or engineers with an increase in the level of controller complexity. The XSG platform provides a virtual FPGA environment for the designing, testing, and development of digital controllers. The integrated platform of MATLAB/Simulink-XSG provides the functionality of automatic HDL code generation that can be further utilized for the straightforward implementation of FPGA-based experimental system prototypes without the additional knowledge of HDL programming. XSG provides a modelling-based design approach for digital system implementation. Therefore, XSG-based system modelling is required for the development of real-time systems using FPGA through automatic HDL code generation. Further, the

recent availability of a model-based FPGA design platform integrated with MATLAB/Simulink provides the functionality of hardware-in-loop (HIL) co-simulation.

2.4. Simulation Methodologies

Simulation modelling solves real-world problems safely and efficiently. It provides an important method of analysis which is easily verified, communicated, and understood. Across industries and disciplines, simulation modelling provides valuable solutions by giving clear insights into complex systems.

2.4.1. Software based platform

Software based platform is a primary approach to design as well as investigate the system. Simulation modelling is computer based and uses algorithms and equations. Simulation software provides a dynamic environment for the analysis of computer models while they are running.The system modelling and design is convenient using the dedicated software based platform available with inbuilt electrical models and blocks. The software based platform can be subdivided into single simulator or hybrid simulator.

A. Individual simulator Environment (ISE)

An electrical system may consist of multiple subsystems that can have distinctive fundamental characteristics. For example, in case of motor drive system, it consists multiple subsystems such as the motor, converter and controller. In single simulator case the entire system model is developed in a unified environment demonstrated in Fig.2.1. Although, single simulator methodology is one of the straightforward approach for system development however it may not duplicate the desired real characteristic considering the individual sub-systems as well as the entire system.

B. Hybrid simulator Environment (HSE)

The hybrid simulator environment: multiple individual software platforms integrated together, can be used for modelling and system development considering the individual sub-systems. In general, the power electronic system consists of subsystems such as electrical circuit and controller. The two dedicated simulator platform

demonstrated in Fig.2.1 that are integrated together can be adopted for modelling to achieve more accurate system characteristic.

2.4.2. Hardware in the loop simulator platform

The hardware in the loop platform is a similar approach as of HSE with a step ahead for authentication and realism for the system development by substituting software environment by an actual hardware. The HIL platforms can be implemented in different combinational aspects such as in case of power electronics drive demonstrated in Fig.2.1.

2.4.3. Hardware platform

After the controller validation in the HIL Platform the controller is implemented using physical devices or electronic circuits as opposed to being done by computer program. A hardware implementation often takes longer to create and that can make it more expensive. HIL platform is usually faster in operation and has the advantage it can easily be tampered with or reprogrammed.

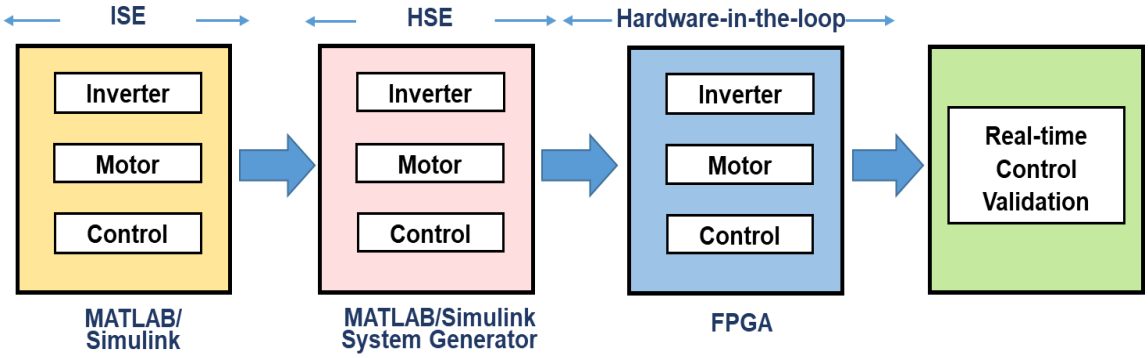


Fig.2.1. Methodologies for system implementation

2.5 Xilinx System Generator

Xilinx System Generator is an FPGA programming tool provided by Xilinx. It is specifically focused on Xilinx FPGAs, enabling the developers to work in Simulink environment and to generate parametrized cores particularly optimized for Xilinx FPGAs. The tool comes built in with Xilinx ISE Design Suite (System Edition) and Xilinx Vivado HL (System Edition). By default, the Xilinx Block set contains over 90 DSP blocks,

ranging from simple adders, multipliers etc. to complex blocks such as Forward Error Correction blocks, FFTs, filters and memories, etc. Some of these blocks also support floating-point DSP. The library provided by Xilinx lists such blocks. Moreover, the System Generator also includes the mcode and Black Box blocks, which can be used to integrate mcode and HDL codes, respectively, directly into the Simulink design environment. The XSG based simulation platform is shown in Fig. 2.2.

The system generator blocks do not automatically convert the Simulink floating-point numbers to fixed-point. Unlike the HDL Coder, where the floating-point numbers are automatically converted to fixed-point, the System Generator utilizes the Gateway In and Gateway Out Blocks to convert from floating point to fixed-point and vice-versa, respectively. The downside to having to use Gateway In and Gateway Out blocks is the potential to make mistakes during this conversion. For example, the designer has to be careful when selecting the number of fixed-point bits, whether the fixed-point number is signed or unsigned as well as the placement of binary point. Additionally, it is also time consuming, for example, when connecting Simulink scopes for design verification, each input to the scope has to be passed through the Gateway Out block in order to convert from fixed-point back to the floating point.

As far as the rest of the modelling design process is concerned, the System Generator works quite similar to HDL Coder, i.e., users drag and drop various blocks into the Simulink environment in order to design the overall system. Users can then use MATLAB scopes and other sinks as well as elements of Sources library to check the design results. Since System Generator is already part of Xilinx ISE or Vivado HS, no additional synthesis tools are required and the users can generate the bit stream directly from within the Simulink environment. To this end, the System Generator token, needs to be added to the design. The System Generator token provides the users with functionality quite similar to HDL Coder's Workflow Advisor, in that it allows users to select specific target workflow and platform. The System Generator also supports "Hardware in the loop" feature, of HDL Coder and HDL Verifier. The Hardware Co-Simulation enables the users to perform tests on real hardware directly from within Simulink.

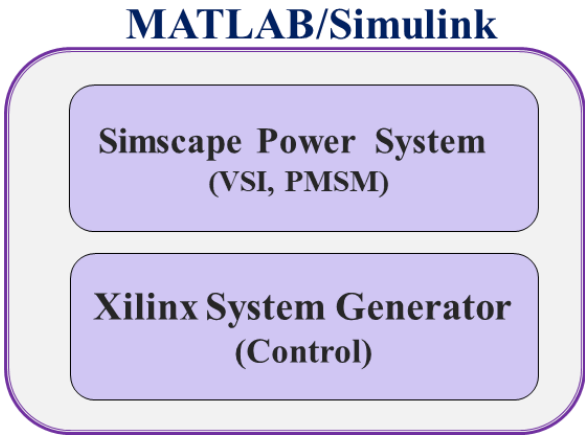


Fig. 2.2 XSG based Implementation

2.6 Hardware-in-loop Simulation

HIL simulation (Software + Hardware) is a technique that is used increasingly in the rapid development and testing of complex real-time embedded systems. The HIL simulation and rapid prototyping methodologies provide an intermediate level of system verification between software simulation and hardware testing. It is considered an effective method to test the performance of any novel controller or any modified controller on a simulator before implementing it on the real time environment. In this approach, the design is deployed to hardware and runs in real-time. However, the surrounding components are simulated in a software environment.

In this work, the HIL co-simulation testing is performed on the XSG-based real-time simulator of FPGA (as a hardware device). The flowchart of the HIL co-simulation using FPGA is shown in Fig. 2.3 with the three-stage validation process. At the initial stage, the controller, VSI system and motor are modelled in MATLAB/Simulink and the performance is verified. Further, controller modelling is developed using the XSG digital platform and the performance is analyzed considering the model of the control using Simulink. The digital modelling of the controller is validated at the later stage through the real-time HIL co-simulation.

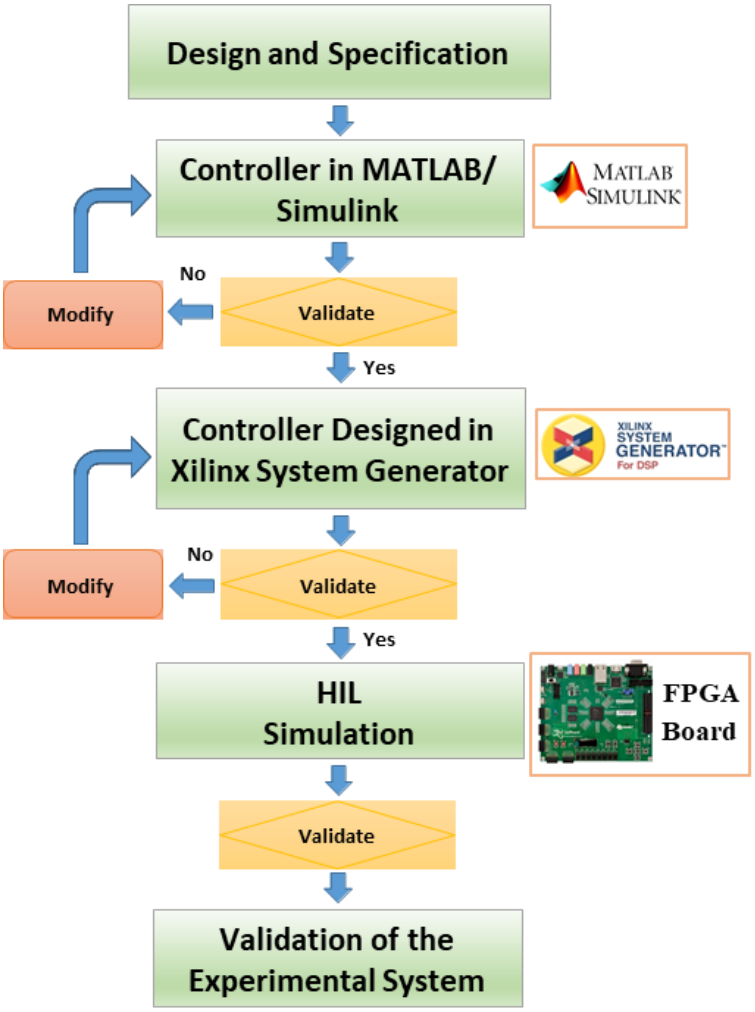


Fig. 2.3 HIL Simulation Flowchart

The HIL co-simulation is considered for validation of the controller by implementing it on the hardware system through the interaction with the software system as shown in Fig. 2.4. In this work, the co-simulation is performed using FPGA as actual hardware by interacting with the computer as shown in Fig. 2.4. Firstly, the modelling of the controller is developed in the XSG and further validation is performed using the co-simulation functionality of the XSG platform. The HIL co-simulation is performed by implementing the FS-MPC in the FPGA through its interaction with the VSI system and motor model in MATLAB/Simulink. The co-simulation prototype block is generated by selecting the appropriate FPGA evaluation board using the XSG token in MATLAB/Simulink. The co-

simulation prototype block enables the MATLAB/Simulink system to interact with the FPGA. The signal ports are assigned in the co-simulation block corresponding to the input signal from Simulink to the XSG and output signal from the XSG to Simulink.

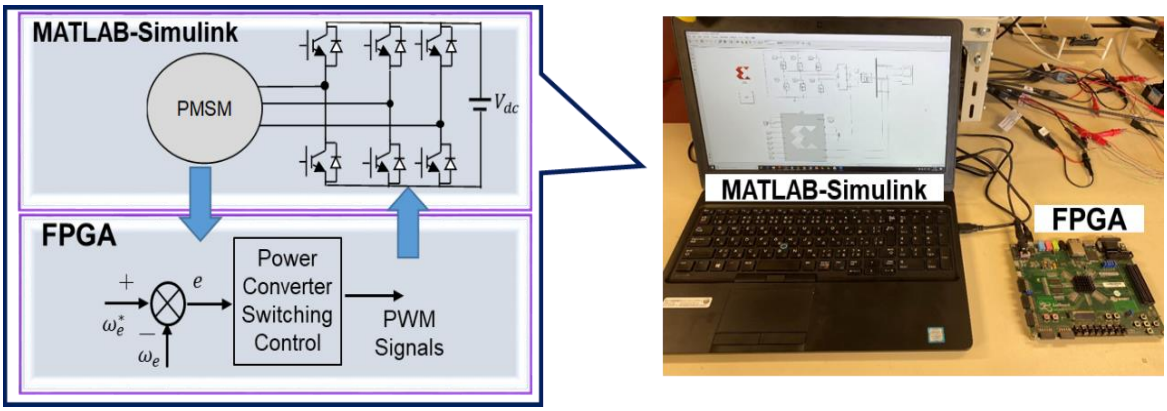


Fig. 2.4 HIL co-simulation methodology

2.7. Suitability of FPGAs for Drive Applications

The dominating digital computing devices for motor control applications are DSPs. Drive industry has already more than 30 year's maturity of DSP applications. Moreover DSP vendors have also a long experience in customizing the microcontroller devices for demanding motor control applications. Despite these facts, using FPGAs has some advantages in terms of computational performance and design issues that make them attractive for research and industrial applications.

An important argument against using FPGAs is relatively longer development time. However, it is not a long term challenge, since there are always more and more skilled engineers in the area of FPGA development. In addition the computer-based design tools are always advancing which can be an effective way for dealing with the complexity of the FPGA programming. Such tools can play significant roles not only for code generation but also for verification and debugging of the code on the target FPGAs. Furthermore, the configurability of FPGAs provides the same level of design convenience as the software in DSPs [89].

Despite the capability of the industry for integrating many digital and analog devices on a single chip, there are some performance criteria which are not cost effective and even not possible to obtain with state-of-the-art of the DSP technology [89]. Dynamic of the current control loop, in particular, for low power servo-drives are very important. Due to the high bandwidth, there are still many applications in which the conventional analog control devices are used. Digital microcontrollers usually provide a lower bandwidth because of the computational time delay. By using FPGAs the digital hardware can be completely dedicated to the control algorithms. It leads to a significantly lower computation time. Therefore in many applications FPGAs can replace analog devices without compromising the performance.

Another application area for FPGAs is the Hardware-In-Loop (HIL) simulation. High computational performance of FPGAs can be beneficial for running real-time models. Because of the short sampling time of electrical drives and power electronics, a precision simulation is usually very time consuming. The parallel processing capability of FPGAs can be very helpful for running computationally intensive models [90], [91].

In addition to all aforementioned applications for which FPGAs provide the only feasible solution, there are some other advantages of FPGA-based systems as alternatives versus conventional DSP systems [89].

2.8. Summery

The DSP technology has three decades maturity for the control system of electrical motors and power electronics. Nevertheless, there are many control algorithms which are too complex to be realized on DSPs or at least it is not cost effective. Increasing logic density and programming tools rise interests in FPGA as an alternative. Hardware programmability of FPGAs allows to fully dedicate the digital system to the control algorithm. Despite the maturity of the DSP technology, diversity of motor control applications makes it difficult to have a universal DSP meeting all requirements. A solution is using FPGAs to have a configurable design.

High logic density and programmability of FPGAs represent extraordinarily high computational performance. Thanks to parallelism and hardware implementation of all tasks, FPGAs are able to manage precise timing requirements which are necessary for real-time systems. There are various tools available for development and verification of FPGA-based designs. Xilinx System Generator is an FPGA programming tool provided by Xilinx. It is specifically focused on Xilinx FPGAs, enabling the developers to work in Simulink environment and to generate parametrized cores particularly optimized for Xilinx FPGAs. It can generate the HDL code automatically and the users can generate the bit stream directly from within the Simulink environment for the real time implementation.

Chapter 3

CONVENTIONAL PMSM DRIVE: FIELD ORIENTED CONTROL

3.1 Introduction

Operation theory of the DC motor shows that the produced torque and the flux can be independently tuned. However, AC machines do not have the same features as the DC motor. This becomes a barrier to AC drives to be widely accepted in the market. The issue was not solved until the 1970s when the FOC technique was first proposed for induction machines. Studies of AC machines showed that the mechanisms of torque production in AC and DC machines are quite similar. With the help of the Park transformation, the current components corresponding to the field-magnetizing flux and torque generation in AC machines can be decoupled orthogonally so that the field-magnetizing flux can be controlled without affecting the dynamic response of the torque and vice versa. This is the basic principle of the FOC. In FOC, the flux and torque of AC machines can be separately controlled as DC motors.

Shortly after it was proposed, FOC was successfully applied to synchronous motors. With the speed and current feedback, PMSM drive with FOC can achieve precise speed control and frees itself from the mechanical commutation drawbacks. Over the years, FOC drives have achieved a high degree of maturity in a wide range of applications. They have established a substantial worldwide market which continues to increase. FOC can be divided into: air gap magnetic field orientated, stator magnetic field oriented, and rotor magnetic field oriented depending on the selected directional magnetic field. For the PMSM, due to the constant magnetic flux of the permanent magnet in the rotor, the rotor magnetic field oriented control is generally adopted. At present, the research and

application objects mainly focus on sinusoidal PMSMs compared with the trapezoidal PMSMs.

3.2 PMSM Mathematical Model

The mathematical model of AC machines is a time-variant, multivariable, nonlinear and coupling system. To obtain excellent control of PMSMs, their mathematical model needs to be established based on the hypotheses below:

(1) Neglecting core saturation, irrespective of core eddy current and hysteresis loss;
(2) The electric conductivity of permanent magnet material is zero;
(3) No damper windings in rotor;
(4) The excitation magnetic field generated by the permanent magnet and the armature reaction magnetic field generated by the three-phase winding are all sinusoidal distributed in the air gap.

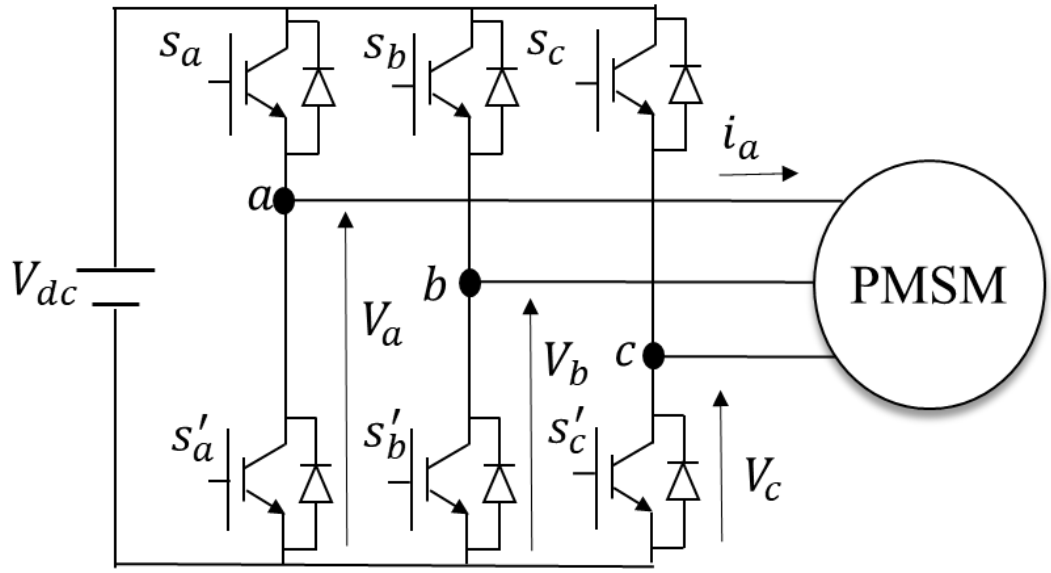


Fig.3.1. Three phase VSI fed PMSM

The power circuit with three phase inverter fed PMSM motor is shown in the Fig.3.1.By defining the following space vector definitions for the stator voltage (v_s), stator current(i_s), and stator flux (ψ_s), respectively,

$$v_s = \frac{2}{3}(v_a + av_b + a^2 v_c) \tag{3.1}$$

$$i_s = \frac{2}{3}(i_a + ai_b + a^2 i_c) \tag{3.2}$$

$$\Psi_s = \frac{2}{3}(\Psi_a + a\Psi_b + a^2 \Psi_c) \tag{3.3}$$

The PMSM stator dynamic equations is described as:

$$v_s = R_s i_s + \frac{d\psi_s}{dt} \tag{3.4}$$

Where, R_s is the stator resistance.

The stator flux linkage $\boldsymbol{\psi}_s$ is generated by the rotor magnets and the self-linked flux produced by the stator currents. This relation is described by

$$\Psi_s = L_s i_s + \Psi_m e^{j\theta_r} \tag{3.5}$$

Where, L_s is the stator self-inductance, ψ_m is the flux magnitude due to the rotor magnets, and θ_r is the rotor position. Inserting (3.5) into (3.4) we obtain

$$v_s = R_s i_s + L_s \frac{di_s}{dt} + j\Psi_m \omega_r e^{j\theta_r} \tag{3.6}$$

Where, $\omega_r = d\theta_r/dt$ is the rotor speed. Multiplying by $e^{-j\theta r}$ and considering the stator voltage and current space vectors in rotor coordinates aligned with the rotor axis $v_s^{(r)} = v_s e^{-j\theta r}$ and $i_s^{(r)} = i_s e^{-j\theta r}$ (3.6) becomes

$$v_s^{(r)} = R_s i_s^{(r)} + L_s \frac{di_s^{(r)}}{dt} + jL_s \omega_r i_s^{(r)} + j\Psi_m \omega_r \tag{3.7}$$

Where, superscript *(r)* denotes rotor coordinates.

$v_s^{(r)} = v_{sd} + jv_{sq}$ and $i_s^{(r)} = i_{sd} + ji_{sq}$

The relation between the stator vectors and the rotating reference frame is shown in Fig.3.2. As the motor inductance varies with the motor angular position therefore the mathematical modeling of the motors is considered on the two phase equivalent circuit (dq).

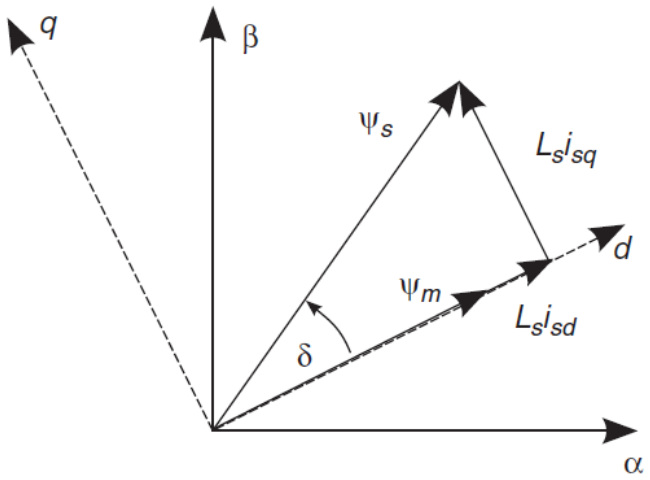


Fig.3.2. Vector diagram of the stator variables and the rotating reference frame

The stator voltage equation in (3.7) on *dq* coordinate can be given as:

$$v_d = R_s i_d + L_s \frac{di_d}{dt} - p_p \omega_r L_s i_q \tag{3.8}$$

$$v_q = R_s i_q + L_s \frac{di_q}{dt} + p_p \omega_r L_s i_d + \psi_m \omega_r \tag{3.9}$$

Where,

$\omega_r = d\theta/dt$ is the mechanical rotor angular speed. Where p_p is the number of pole pair of the motor.

The electromagnetic torque produced by the motor is expressed bellow that depends upon stator quadrature component current and magnitude of the flux.

$$T_e = \frac{3}{2} p_p \psi_m i_q \tag{3.10}$$

The mechanical dynamics of the motor can be given as:

$$\frac{d\omega_r}{dt} = \frac{1}{J}\left(T_e - T_l\right) - \frac{B}{J}\omega_r \tag{3.11}$$

J is the motor inertia, B is the friction coefficient, and T_l is the load Torque. The rotor electrical angular speed ω_e is given by:

$$\omega_e = p_p \omega_r \tag{3.12}$$

The mathematical modeling for both the electrical and mechanical dynamics of the motor is illustrated in the Fig.3.3.

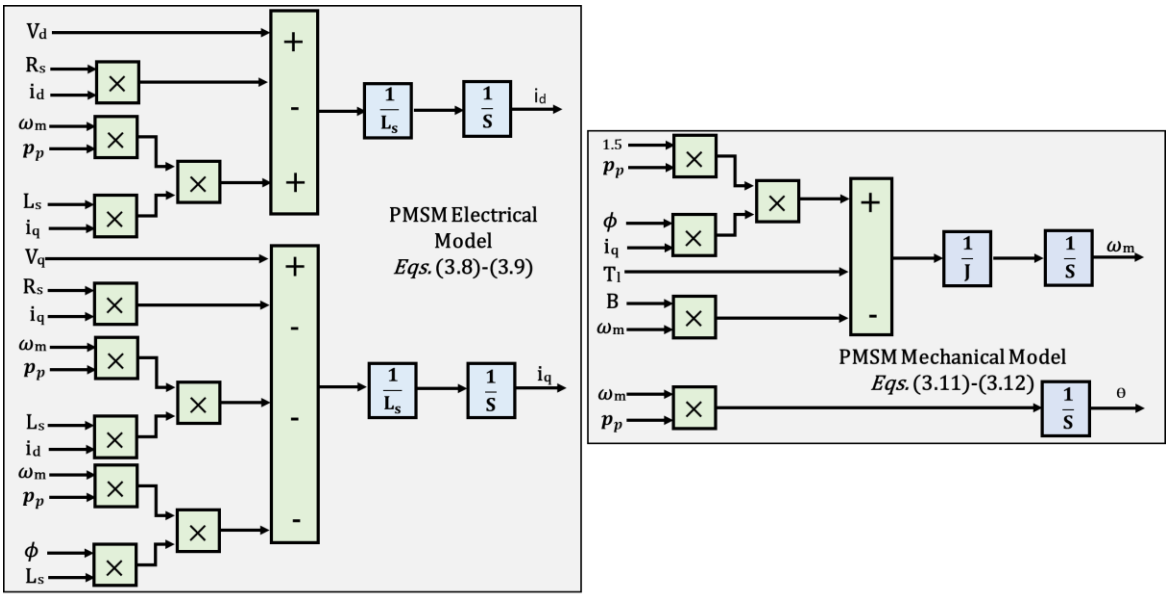


Fig.3.3 PMSM Model

3.3. Field Oriented Control

The FOC for the speed control of the PMSM is presented in the Fig.3.4. The FOC is a simple vector control which can control both the phase as well as the phase current magnitude of the motor. The implementation methodology of the control is includes, speed control loop then current control loop and finally the generation of the switching signal for the power converter.

The speed control loop evaluate the reference quadrature axis current i_{qref} to control the current magnitude corresponding to the motor load condition. As the motor torque for a surface PMSM (SPMSM) depends upon only the quadrature axis current so the direct axis current i_{dref} is kept zero. This method is to control the direct axis current to be zero, so there is no direct axis armature reaction. Regardless of the SPMSM or interior PMSM, the torque is only proportional to the quadrature axis current, and the control structure is simple.

The disadvantage is that the motor power factor decreases as the load increases. The i_{qref} in the stationary reference frame is evaluated by feeding the speed error signal through PI controller. The equations involved for the generation of the reference current signal is given as:

$$i_q^* = \left(k_{p\omega} + \frac{k_{i\omega}}{s} \right) \omega_{er} \tag{3.13}$$

Where, S is the Laplace operator. The ω_{er} is given by:

$$\omega_{er} = \omega^* - \omega_r \tag{3.14}$$

The i_d and i_q current can be obtained from the motor sensed three phase current by using the following matrix.

$$\begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} \tag{3.15}$$

$$\begin{bmatrix} i_d \\ i_q \end{bmatrix} = \begin{bmatrix} \cos\theta & \sin\theta \\ -\sin\theta & \cos\theta \end{bmatrix} \begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} \tag{3.16}$$

The motor current i_d and i_q are compared to the reference current generated from the speed control loop. These error signals are converted to their equivalent voltages by using the PI controller. The current control unit evaluates the reference voltages corresponding to the current for the motor speed control. The following equations represents the d-q axis reference voltage equations:

$$v_d^* = \left(k_{pd} + \frac{k_{id}}{s} \right) i_{der} \tag{3.17}$$

$$i_{der} = i_d^* - i_d \tag{3.18}$$

$$v_q^* = \left(k_{pq} + \frac{k_{iq}}{s} \right) i_{qer} \tag{3.19}$$

$$i_{qer} = i_q^* - i_q \tag{3.20}$$

These reference voltage vectors are converted to the reference three phase voltages by using following equations.

$$\begin{bmatrix} v_\alpha \\ v_\beta \end{bmatrix} = \begin{bmatrix} cos\theta & -sin\theta \\ sin\theta & cos\theta \end{bmatrix} \begin{bmatrix} v_d \\ v_q \end{bmatrix} \tag{3.21}$$

$$\begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & 0 \\ -\frac{1}{2} & \frac{\sqrt{3}}{2} \\ -\frac{1}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} v_\alpha \\ v_\beta \end{bmatrix} \tag{3.22}$$

For the final step the reference signal is compared to the triangular wave for the generation of the switching signal.

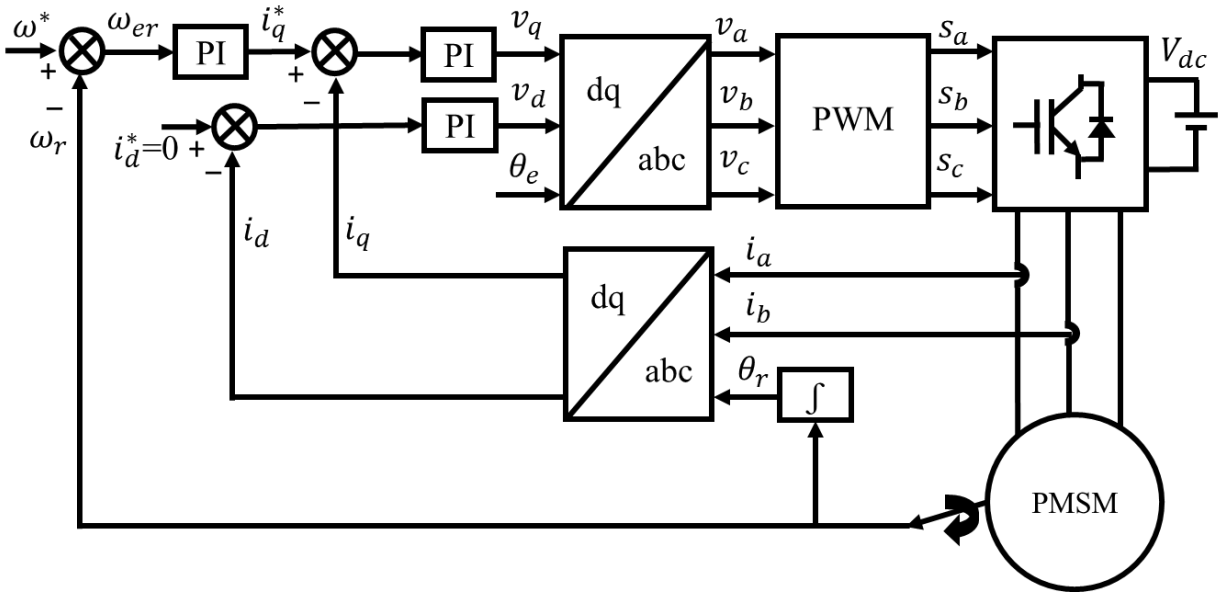


Fig.3.4 FOC based PMSM drive system

3.4 Controller Designing in XSG

XSG is a digital designing tool integrated with the MATLAB/Simulink and can be used for the FPGA-based system development. The model-based design in XSG has the functionality for automatic generation of the hardware description language (HDL) code that can be readily used for the real-time operation of FPGA-based system. FOC-based speed control of the PMSM drive system is designed and modelled in MATLAB/Simulink using XSG blockset. The modelling of the FOC is considered in three parts which is explained in detail.

3.4.1 Outer Speed Control Loop

The outer control loop of the FOC consists of a PI controller to regulate the motor speed. The implementation of the speed controller in XSG is presented in the Fig.3.5. The PI controller implementation in FPGA using discrete-time domain platform of XSG, requires the discretization of dynamic Equation (3.13). To get a discrete-time model it is necessary to use some discretization methods. For first-order systems it is useful, because it is simple. There are several method are present to obtain the discrete-time-model. In this work to approximate the derivatives the Euler forward method is used, that is given as:

$$\frac{dx}{dt} = \frac{i(k+1) - i(k)}{T_S}$$

Where, T_s is the sampling time. However, when the order of the system is higher, the discrete-time model obtained using the Euler method is not so good because the error introduced by this method for higher order systems is significant. For these higher order systems, an exact discretization must be used. The discretized equation for the PI control is presented as:

$$\begin{aligned} i_q^*(k) &= K_{p\omega}\omega_{er}(k) + g_\omega(k) \\ g_\omega(k) &= g_\omega(k-1) + K_{i\omega}T_S\omega_{er}(k) \end{aligned} \tag{3.23}$$

where i_q*(k) and $\omega_{er}(k)$ are the reference q axis stator current and speed error at the instant k. $g_\omega(k)$ is the output of the integral control at the instant k. T_s is the sampling time.

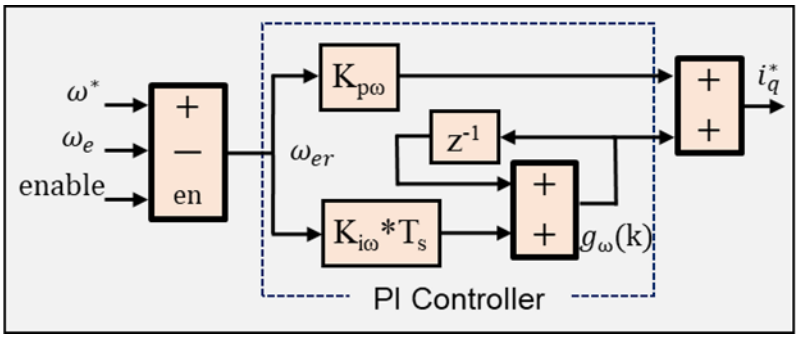


Fig.3.5 Speed control loop

3.4.2. Inner Current Control Loop

The control of the dc motor is easier as the speed is directly proportional to the current. However, in case of the ac motor in order to achieve similar kind of behavior, the co-ordinate transformation is an essential part of the controller design. Initially, abc-dq transformation is performed using an enable signal for conversion form three phase to two phase system abc-αβ, and subsequently, the conversion of two-phase system to synchronously rotating frame αβ-dq transformation using sin-cos shown in the Fig.3.6.

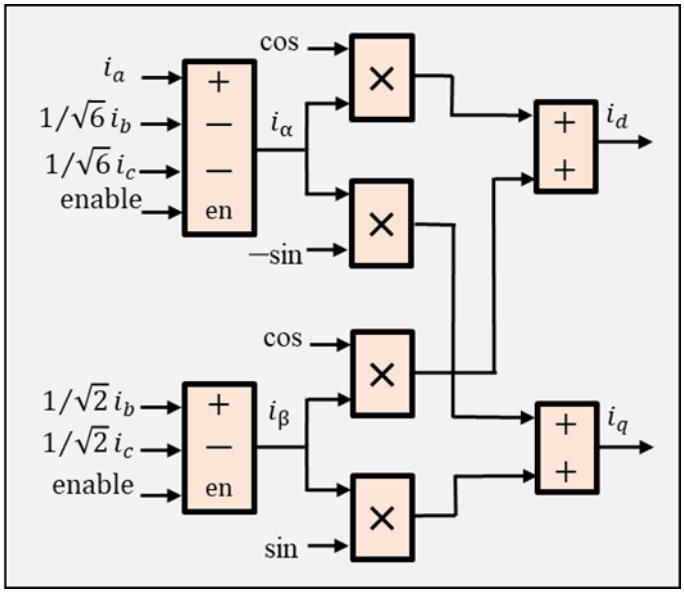


Fig.3.6 abc-dq conversion

In the inner current control loop, two PI controllers are used as shown in Fig.3.7 to generate an equivalent voltage quantity for generation of switching signals. Similar to the speed PI controller, the current PI controller is represented for dq quantity in the discrete-time domain as:

$$v_d(k) = K_{pd} i_{der}(k) + g_d(k)$$
$$g_d(k) = g_d(k-1) + K_{id} T_s i_{der}(k) \quad (3.24)$$

$$v_q(k) = K_{pq} i_{qer}(k) + g_q(k)$$
$$g_q(k) = g_q(k-1) + K_{iq} T_s i_{qer}(k) \quad (3.25)$$

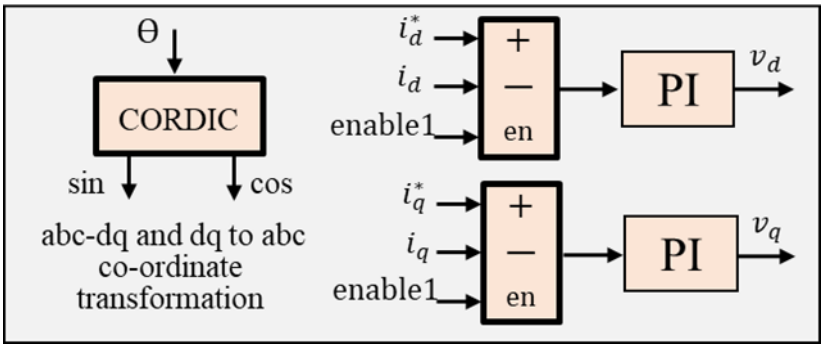


Fig.3.7. Current PI control

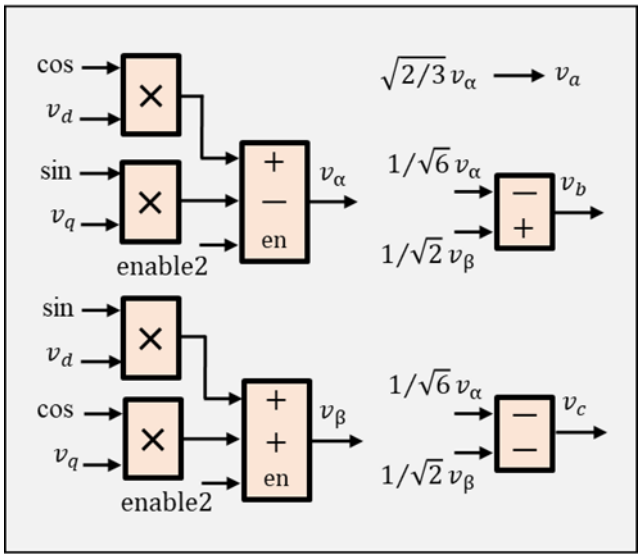


Fig.3.8. dq-abc conversion

Where, $v_d(k)$ and $v_q(k)$ are the stator reference voltage at the instant k. $i_{der}(k)$ and $i_{qer}(k)$ are the current error signal at the instant k. g_d (k) and g_q (k) are the output of the integral control at the instant k. Further, dq-abc transformation is performed, as shown in Fig.3.8 to convert into three phase voltage quantity for the generation of the switching signal.

3.4.3. Switching Signal Generation

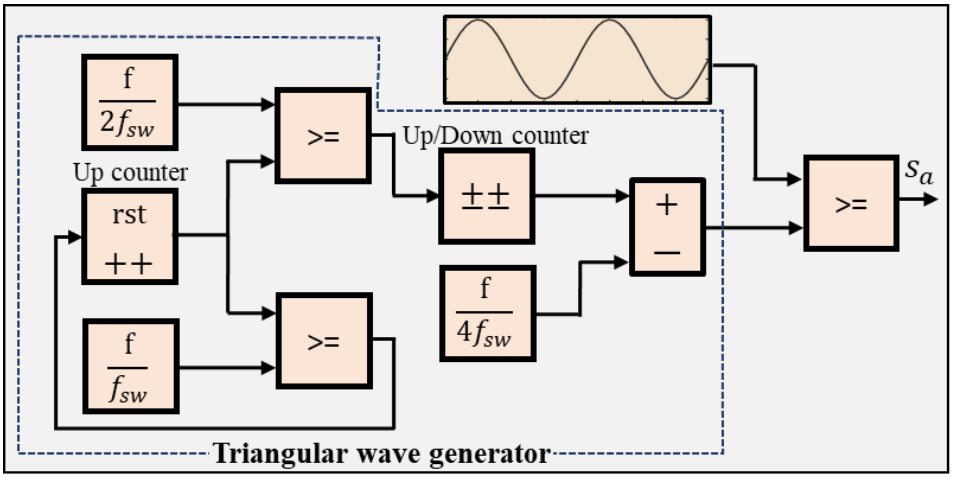


Fig.3.9. Switching pulse generation.

The Sine triangle pulse width modulation (SPWM) is considered for the generation of the switching signal. The switching signal is generated using a PWM technique that requires a carrier wave and modulating wave. The triangular waveform as a carrier signal of frequency f_{sw}, is generated by using the fundamental blockset of the XSG, as shown in Fig.3.9. The sinusoidal three phase voltage waveform as a modulating signal is compared with the triangular wave to generate the switching pulses for a three-phase inverter system. A free running up counter block is used to generate a ramp signal. If the counter count for the ramp signal is greater than the desired triangular wave frequency the counter will be reset. Afterwards, the counter output is compared to that of the half of the triangular wave frequency. Finally, an up/down counter is used to perform the increment when the value is 1 and decrement when the value is zero. For the generation of the switching signal, the carrier wave is compared to that of incoming reference voltage signal and updated immediately. The Inverter used for the experimental validation has an inbuilt inversion

circuit with dead time compensation for the PWM signal. Therefore, the switching signals are only generated for the upper half power devices of the inverter.

3.5 FPGA System Implementation

The feedback control implementation of the PMSM drive system requires sensing of the control parameters: motor speed and current. Further, the sensed parameters are needed to feed to the control environment. Analog to digital converter (ADC) is used to feed the sensed control parameters to the digital control environment. PMSM drive system in Fig.3.10 is designed and developed using the digital control environment of FPGA. The encoder unit has the purpose to sense the rotor angular speed and angular position by generating pulses with a resolution of 2048 counts per revolution. The position and speed detector calculates the speed and rotor positions using the encoder pulses. The motor current sensed through a current sensor and fed to the FPGA through an ADC as shown in Fig.3.10. These currents are further passed through the PI controller unit. The control unit along with the ADC- digital to analog converter (DAC) interface unit and PWM generation unit is programmed to the FPGA board. The DAC interface unit is used to convert the controlled parameters into an analog signal, and it is measured and recorded through memory Hi-corder for monitoring and validation.

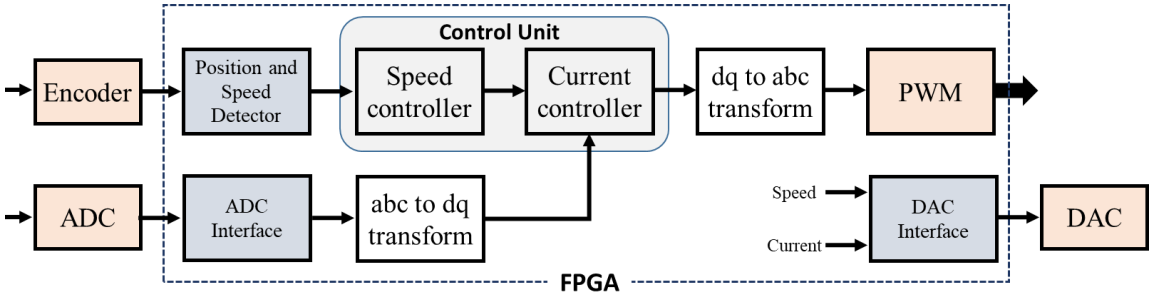


Fig.3.10. Field programmable gate array (FPGA) implementation of the PMSM drive system.

3.5.1. ADC Interface

An interface program is developed for the operation of ADC to feedback the signal to FPGA. The schematic diagram in Fig.3.11 represents the ADC interfacing and pin

configuration of PMOD (Peripheral Module) AD1. PMOD AD1 is consisting of a 12-bit, two-channel AD7476A ADC with maximum possible sampling rate up to 1MSPS. PMOD AD1 has six input pins that is for two analog input signals (i_a and i_b) with their respective ground pins and a power supply pin (VCC) with its respective ground pin (GND). Similarly, the PMOD AD1 has six output pins that are connected to the FPGA, consisting of a clock pin (Clk), chip select (CS) pin, two digital data output pins (D_1 and D_2) and a VCC with its respective GND.

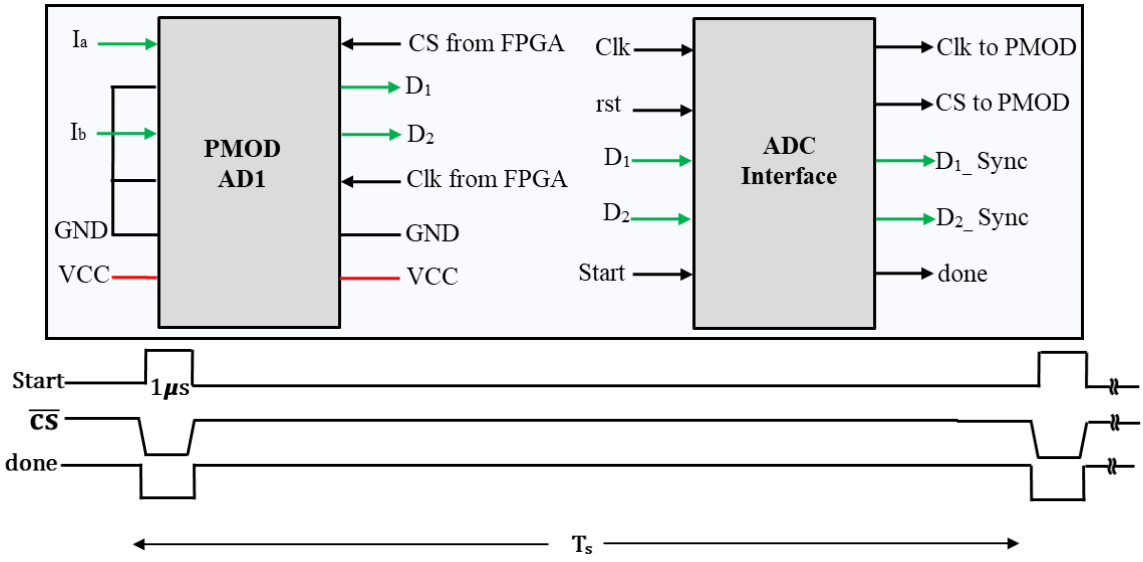


Fig.3.11. PMOD AD1 with an analog to digital converter (ADC) interface.

Clk and CS signals are provided from FPGA using the ADC interface program block as shown in Figure 3.11. The conversion and data acquisition process is governed by the CS signal. The falling edge of the CS initializes the sampling of data as well as the data conversion. The digitized data D_1 and D_2 are synchronized at the rate of sampling frequency using the start signal through the ADC interface and it generates the CS signal corresponding to the start signal condition. Once the acquisition following the sampling as well as conversion of the analog data is completed, it generates a done signal as shown in Fig.3.11. The AD converter works at 1MSPS and following the requirement for the implementation of the control algorithm the sampling frequency is specified using the start signal.

3.5.2. Timing Diagram of Closed Loop

The sampled digitized data of the feedback control parameters are further used for the control algorithm of motor drive system. The control algorithm consists of a speed control unit, current control unit and PWM generation unit. The control algorithm execution is required to be completed within a pre-specified sampling time interval. The crucial factors are sampling time as well as execution of control algorithm in a synchronized way to generate the PWM switching signals. The sampling time at least should be half the carrier time (minimum sampling frequency should be double of the carrier frequency) as represented in Fig.3.12 a. In addition, the sampling frequency can be taken higher; however, the impact of lower sampling time for the same carrier frequency may not always be advantageous.

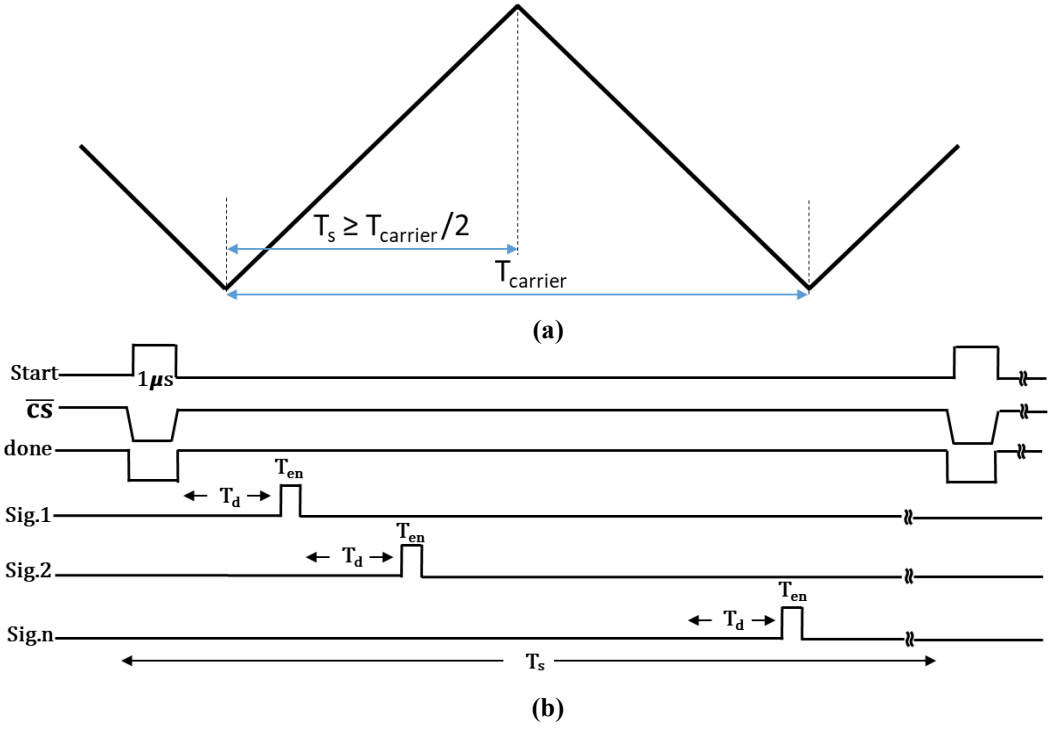


Fig.3.12. Control loop timing criteria: (a) sampling time criteria with respect to carrier frequency (b) execution timing diagram.

The control algorithm is required to be executed in a sequential way as the output of the outer control loop generates the reference quantity and feeds to the inner control loop. The performance of the system is dependent on the controller bandwidth. The inner control

loop has a dominant impact on the outer control loop; therefore, the bandwidth of the inner control loop should be higher to accommodate the bandwidth of the outer control loop. Furthermore, the execution timing can be crucial and may have significant impact on the system's performance. The enabled signals (done, sig.1–sig. n) are generated with on time T_{en} for the execution of control algorithm. A buffer delay time of T_d is inserted for the successive enabled signals to avoid overlapping.

3.5.3. Time Synchronization

A time synchronization for the execution of entire control algorithm is crucial for the system performance. As the output of one unit is responsible for the next, a sequential time synchronization is used to perform the computation of the control algorithm within a sampling time.

The timing diagram in Fig.3.12b is used for the implementation of the control algorithm in the FPGA. The start signal width is defined by sampling time T_s with on time of 1µs following the throughput time of ADC. Consequently, the done signal was switched to a high state following the quite time of 400 ns after the start signal switched to the low state. Following the done signal, the enabled signals are generated for the time-synchronized execution of the control algorithm.

There are various possibilities to generate the enabled signals to perform time-synchronization corresponding to the sampling time. In this study, enabled signals with on time T_{en} of 0.5 µs and a buffer delay time T_d of 2.5 µs in between consecutive signals are considered for the time-synchronization analysis of the control algorithm. The enabled signal (done) enables the speed controller loop as well as abc to dq conversion simultaneously to perform parallel computation as shown in the Fig.3.13. Further, a methodological approach is considered by using the different combination of enabled input signals for the computation of the current controller unit and dq to abc conversion. There are three cases considered for the analysis of the effect of the time synchronization, as shown in the Fig.3.14, for the computation of current controller unit and dq to abc conversion.

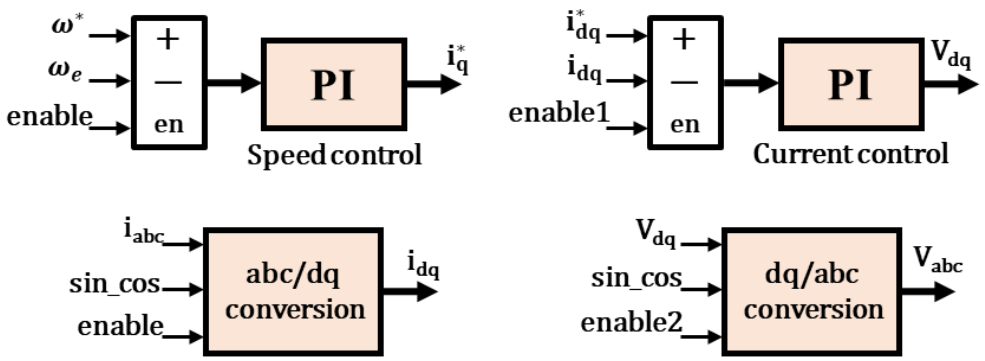


Fig.3.13. Time synchronizations for the system implementation.

Case I:

In case I, the done signal enables the speed PI controller and abc–dq conversion. Further, the enable1 signal with T_{en} of 0.5 µs and T_d of 2.5 µs from the done signal is used to enable the current PI control. Similarly, the enable 2 signal with T_{en} of 0.5 µs and T_d of 5.5 µs from the enable1 signal is considered to enable the dq–abc conversion. The timing diagram executing case I is represented in Fig.3.14a.

Case II:

In this case, similar to case I, the done signal enables the speed PI controller and abc–dq conversion, and the enable1 signal with T_{en} of 0.5 µs and T_d of 5.5 µs from done signal is used to enable the current PI controller. Further, the enable2 signal with T_{en} of 0.5 µs and T_d of 5.5 µs from the enable1 signal enables the dq–abc transformations. The timing diagram for case II is shown in Fig.3.14b.

Case III:

Similar to case I and II the enable1 with T_{en} of 0.5 µs and T_d of 8.5 µs is used as an enable signal for the current controller loop and the enable2 with T_{en} of 0.5 µs and T_d of 5.5 µs enables the dq to abc transformation. The timing diagram corresponding to case III is shown in the Fig.3.14c.

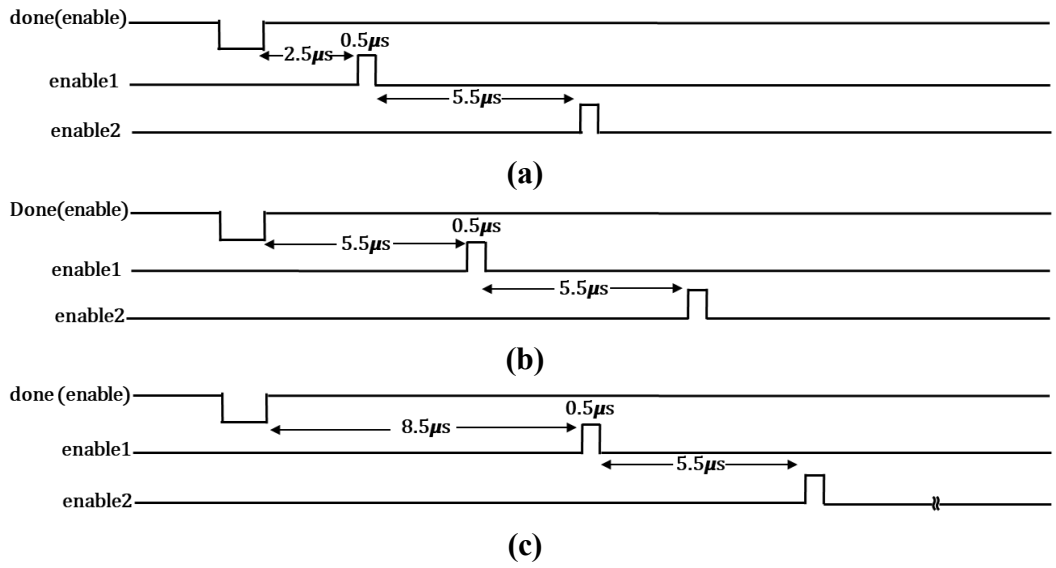


Fig.3.14. Timing diagram considering different case (a) Case I, (b) Case II, (c) Case III.

3.6. Experimental Results and Discussion

An experimental system is developed as shown in Fig.3.15 for the analysis and validation of the time synchronization for the FPGA-based PMSM drive system. The three cases of time synchronization methodology as discussed in Section 3.5.3 are considered for feedback control loop analysis. Sampling frequencies of 25, 50 and 100 kHz are used for the extensive analysis of impacts due to time synchronization. The delay time for case II and case III is more than of 10 μs; therefore, only case I is considered corresponding to the sampling frequency of 100 kHz. A step change in speed reference and motor load condition (load disturbance) is introduced to demonstrate the system performance under transient conditions and examine the effect of time synchronization corresponding to different sampling frequencies. The system parameters and the component specifications are explained in the Tables 3.1 and 3.2. The sampling frequency of the speed controller is same as the current controller. K_p and K_i value for both the speed controller and the current controller are kept constant for all the cases as explained in the Table 3.3. However, considering the different sampling frequency, the sampling time T_s is multiplied with the K_i. The clock frequency considered for the FPGA-based system implementation is 100 MHz.

Table 3.1. System parameters.

Parameters	Values
Dc Voltage V_{dc} [V]	80
Motor rated power [W]	400
Rated torque T_e [Nm]	1.27
Stator resistance R_s [Ω]	0.96
Stator inductance L_s [H]	4.3×10^{-3}
Permanent magnet flux φ [Wb]	0.047
Rotor inertia J [Kg-m^2]	5.3×10^{-5}
Coefficient of viscous friction B [Nm/(rad/s)]	1×10^{-5}
No of pole pairs [p_p]	4

Table 3.2. Specifications of the system.

Components	Specifications
Three phase VSI	STEVAL-IHM023V3, 1 kW
DC voltage supply	ST5360318
Three phase rectifier	S15VT60-4000
Electronic load	LSA-165
Back EMF load	PR-18-5A
Current sensor	ACS723
Isolator	ADuM3440
ADC	PMOD AD1
DAC	PMOD DA4
FPGA board	ARTY Z7-Xc7z020

Table 3.3Controller parameters.

Controller Parameters	Values
$K_{p\omega}$	0.45
$K_{i\omega}$	30
K_{pd}, K_{pq}	5
K_{id}, K_{iq}	20

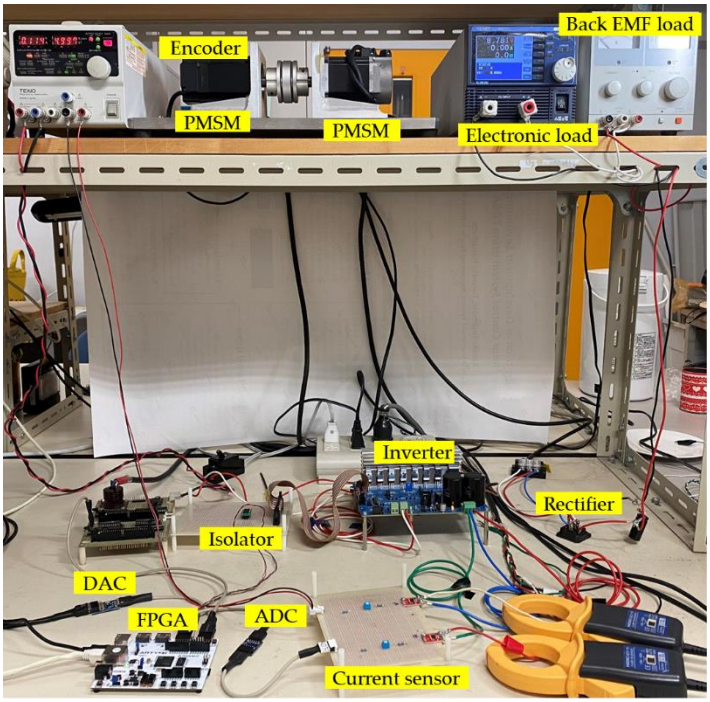


Fig.3.15. Experimental Setup.

The no load speed response corresponding to the motor startup and stop is shown in the Fig.3.16. The speed reference is changed from 0 to 300 rpm (start-up) and 300 to 0 rpm (stop).

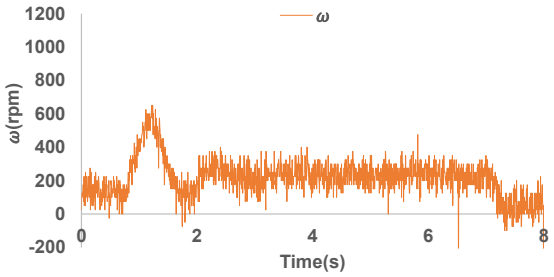


Fig.3.16. Motor speed response.

3.6.1. Change in Reference Speed

The motor system can go under the condition of speed change, and the transient performance of the motor drive system is of concern to attain the new speed smoothly with

a lower settling time. A step change in the reference speed from 900 to 1500 rpm (low to high speed) and 1500 to 900 rpm (high to low speed) is considered to demonstrate and analyze the performance for time synchronization cases as well as sampling frequencies. The switching frequency of 5 kHz is used for the power devices of the inverter corresponding to different sampling time.

The speed regulation of PMSM in Fig.3.17-19 is demonstrated for the sampling frequency of 25, 50 and 100 kHz. The settling time performance of speed regulation is better for 25 and 50 kHz as compared to 100 kHz for the case I of time synchronization. Further, the speed regulation performance has improved in case II and case III for 50 kHz. The settling time performance of speed regulation is summarized in Table 3.4 in terms of time required to attain the steady state.

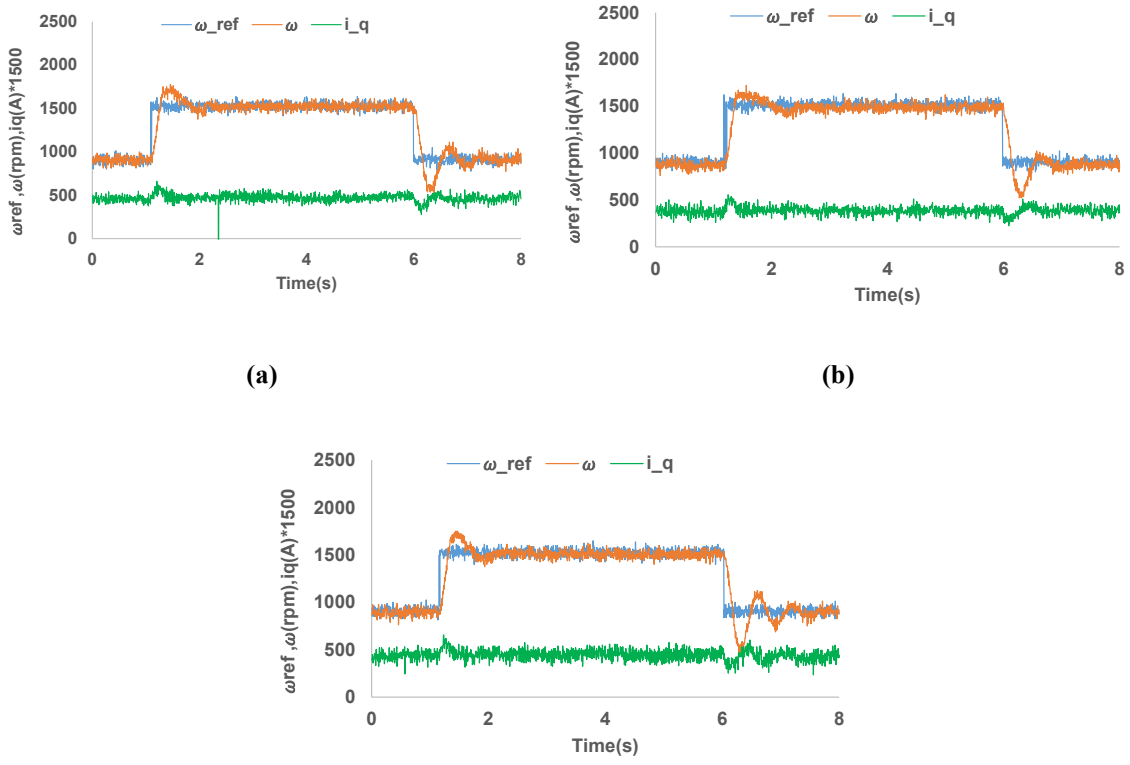
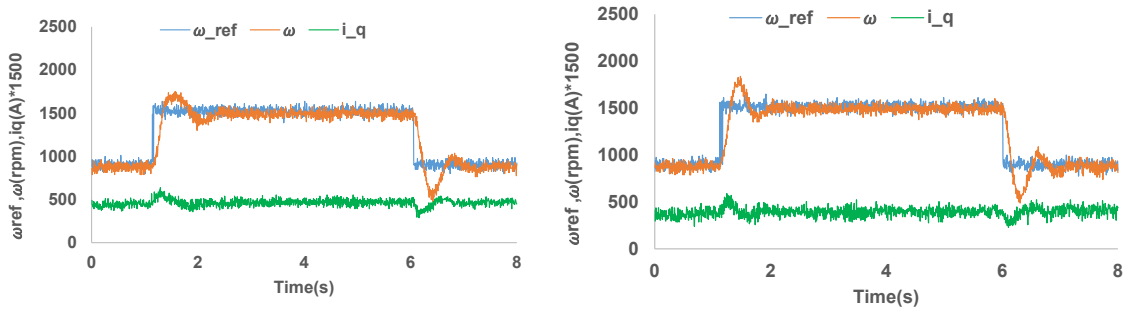
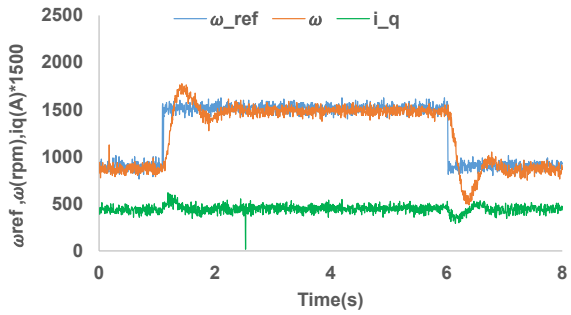


Fig.3.17. Speed response of PMSM at 25 kHz sampling frequency (a) case I, (b) case II and (c) case III.



(a) **(b)**



(c)

Fig.3.18 Speed response of PMSM at 50 kHz sampling frequency (a) case I, (b) case II and (c) case III.

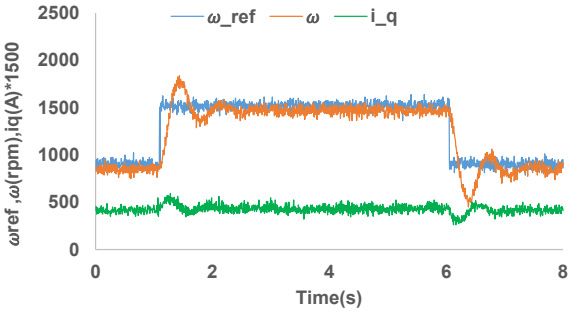


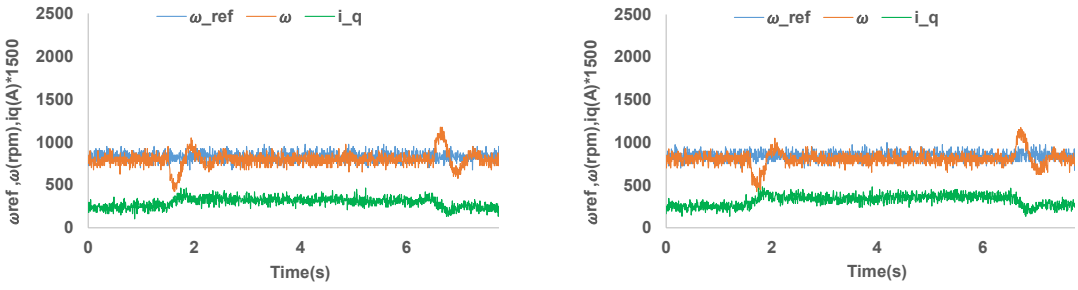
Fig.3.19. Speed response of PMSM at 100 kHz sampling frequency (case I).

Table 3.4 Speed response corresponding to the change of reference speed.

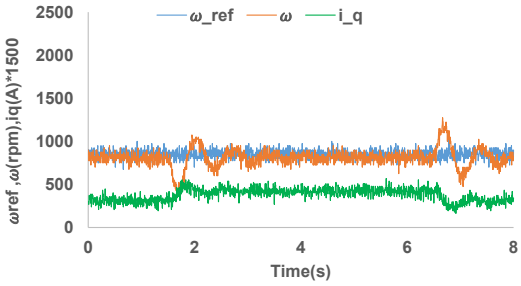
Sampling Frequency (kHz)	Case I		Case II		Case III	
	Low-High	High-Low	Low-High	High-Low	Low-High	High-Low
25	1 s	1.1 s	1.5 s	1.1 s	1.05 s	1.5 s
50	1.25 s	0.7 s	1 s	0.9 s	1.1 s	0.8 s
100	1.5 s	1.2 s	-	-	-	-

4.6.2. Change in Load Condition

The motor system can go under the load disturbance condition as well, and the transient performance of motor drive system is of concern to attain the desired reference speed smoothly with a lower settling time. A step change in the electronic load to introduce a load disturbance is employed that ultimately results in a motor current change from 0.5 to 1 A (low to high) and 1 to 0.5 A (high to low). The switching frequency of 5 kHz is used to analyze the system behavior. The speed regulation of PMSM under load disturbance in Fig.3.20-22 is demonstrated for the sampling frequency of 25, 50 and 100 kHz. The settling time performance of 100 kHz sampling frequency is best for time synchronization in case I from low to high as well as high to low. Further, the speed regulation performance has improved in case II and case III for 50 kHz compared to 25 kHz and become almost same as performance of 100 kHz in case I. The settling time performance of speed under load disturbance is summarized in Table 3.5 considering the time required to attain the steady state.

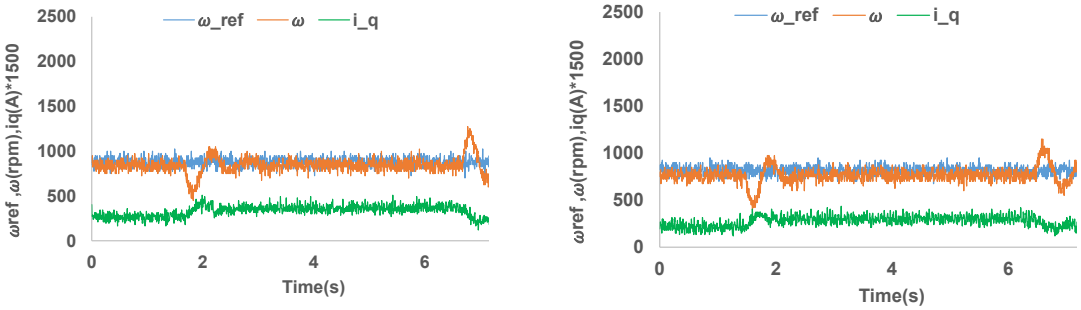


(a) **(b)**

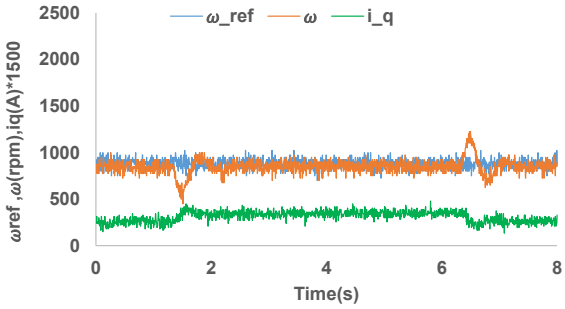


(c)

Fig.3.20. Speed response of PMSM at 25 kHz sampling frequency (a) case I, (b) case II and (c) **case III.**



(a) **(b)**



(c)

Fig.3.21. Speed response of PMSM at 50 kHz sampling frequency (a) case I, (b) case II and (c) case III.

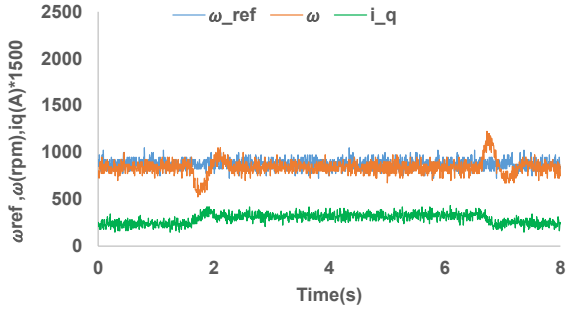


Fig.3.22. Speed response of PMSM at 100 kHz sampling frequency case I.

Table 3.5.Speed response corresponding to the change of load disturbance.

Sampling Frequency (kHz)	Case I		Case II		Case III	
	Low-High	High-Low	Low-High	High-Low	Low-High	High-Low
25	1.5 s	1.3 s	1.3 s	1.1 s	2 s	1.6 s
50	1.3 s	1.15 s	1.1 s	1 s	1 s	0.9 s
100	0.9 s	0.7 s	-	-	-	-

3.6.3. Effect of Sampling Frequency on Speed Control Loop

The mechanical response of the motor is slower compared to that of the electrical response of the motor. Therefore, the sampling rate of the speed controller is slower than that of the current controller. The sampling rate of the encoder considered for the experimental validation is 1 kHz. Considering the sampling rate of the encoder the minimum sampling frequency that can be consider for the implementation of the speed control loop is 1 kHz.

The motor speed response corresponding to the speed controller sampling frequency 1 kHz for the change in the speed reference from 900 to 1500 rpm (low to high) and 1500 to 900 rpm (high to low) is shown in the Fig.3.23. The motor speed response corresponding to change in the load disturbance that results in motor current change from 0.5 to 1 A is shown in Fig.3.24. In order to compare the effect of the sampling frequency on the speed controller the motor speed response with sampling frequency 1 kHz is compared to the 50

kHz sampling frequency. The current controller sampling frequency is considered as 50 kHz for both the cases.

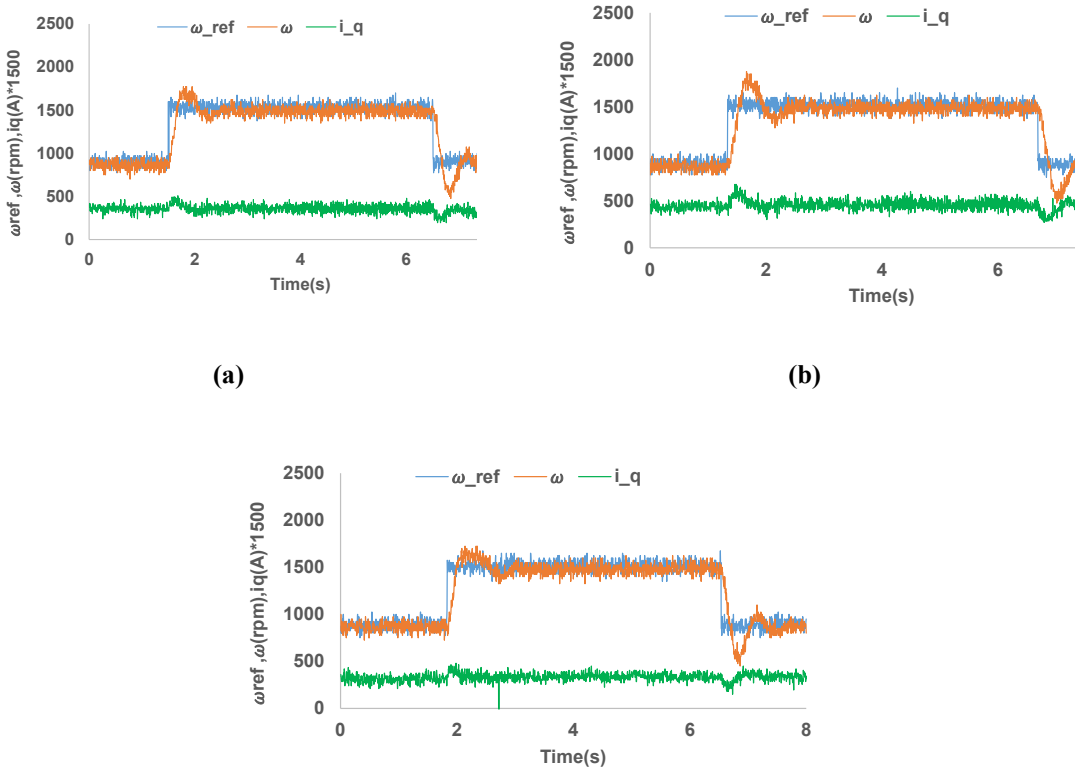
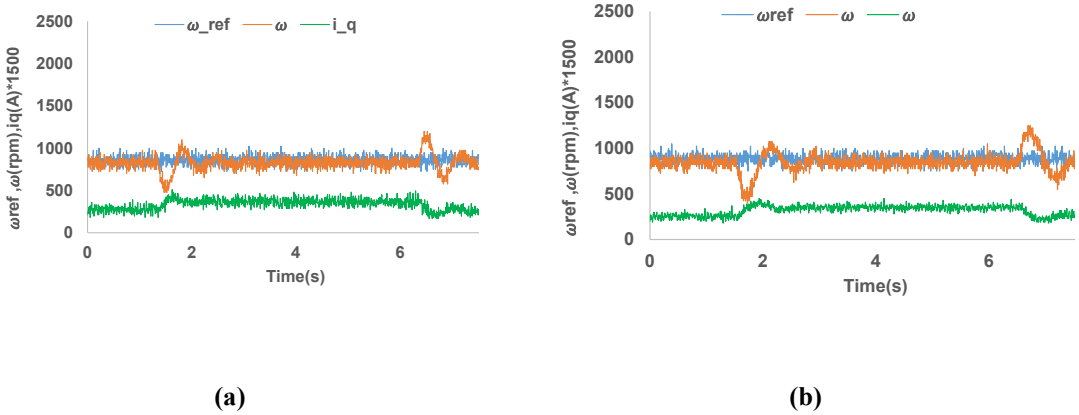
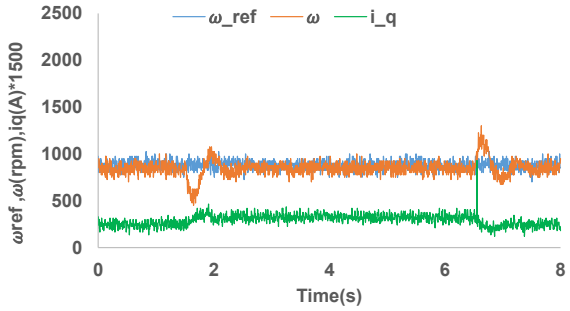


Fig.3.23. Speed response of PMSM (a) case I, (b) case II and (c) **case III.**





(c)

Fig.3.24. Speed response of PMSM (a) case I, (b) case II and (c) **case III.**

The settling time required for the speed response to reach the steady state value is summarized in Table 3.6 for the change in the speed reference and in Table 3.7 for the change in the load torque disturbance corresponding to both speed sampling frequencies of 1 and 50 kHz. The transient response for the sampling frequency of 50 kHz is slightly better compared to the 1 kHz for both change in the speed reference and change in the load torque disturbance. Moreover, case III has a better response for the speed sampling frequencies of 1 and 50 kHz.

Table 3.6. Speed response corresponding to the change of speed reference.

Speed Controller Sampling Frequency (kHz)	Case I		Case II		Case III	
	Low-High	High-Low	Low-High	High-Low	Low-High	High-Low
1	1.1 s	0.8 s	1.2 s	1.2 s	1.2 s	0.9 s
50	1.25 s	0.7 s	1 s	0.9 s	1.1 s	0.8 s

Table 3.7. Speed response corresponding to the change of load disturbance.

Speed Controller Sampling Frequency (kHz)	Case I		Case II		Case III	
	Low-High	High-Low	Low-High	High-Low	Low-High	High-Low
1	1.35 s	1.2 s	1.45 s	1.3 s	1.1 s	0.9 s
50	1.3 s	1.15 s	1.1 s	1 s	1 s	0.9 s

3.6.4. System Performance in Terms of THD

The controller performance (three-phase current harmonics) depends up on the switching frequency at which the power devices are operating as well as on the sampling frequency at which the digitized sampled data are coming. Therefore, different switching frequencies corresponding to the different sampling frequencies are considered to examine and analyze the controller performance. The sampling frequency for the system should be double or more than double the switching frequency and is considered as the fundamental criteria. The combinations of the switching frequency and sampling frequency are exercised to investigate the system performance as shown in the Table 3.8 considering case I of the time synchronization.

The current ripples are presented in the form of total harmonic distortion (THD). The lower switching frequency performance in terms of THD has improved drastically corresponding to an increase in sampling frequencies. Nevertheless, the higher switching frequency results in higher switching losses of the power devices and high sampling frequency demands the high-speed ADC to feedback the data samples at a higher rate. The advancement in digital technology with cost reduction trend can be vital in this aspect.

Table 3.8. Comparison of total harmonic distortion (THD).

Switching Frequency (kHz)	Sampling Frequency (kHz)	%THD
5	10	20
	25	7.5
	50	4.5
	100	3.57
10	25	10.2
	50	3.7
	100	2.25
25	50	2.6
	100	1.52
50	100	2.5

3.7 Summery

The proportional-integral (PI) based control for the motor drive system is commonly used in the industrial applications. However, the motor drive system development and prototyping is a tedious task especially considering a field programmable gate array (FPGA) based real-time system implementation. In addition, the time-synchronization of feedback control loop is another vital aspect concerning sampling time for discrete-time controller. This chapter presents an FPGA based design and development of PMSM drive system considering the impact of time-synchronization for feedback control loop corresponding to sampling frequencies. A step by step and case by case time synchronizations methodology is considered to analyze the repercussion of sampling frequencies corresponding to feedback control loop synchronization. The harmonics in motor current is also taken into account for different switching frequencies and sampling frequencies correspondingly. Furthermore, a step change in reference speed as well as load disturbance is introduced to investigate the transient/dynamic behavior of the system. The controller is developed in the Xilinx system generator (XSG) environment integrated with the MATLAB/Simulink for the FPGA-based experimental system implementation.

The time synchronization of system control corresponding to sampling frequencies having significant impact on motor performance under transient operation. The controller demonstrates better performance under change of speed reference for case II and Case III with sampling frequency of 50 kHz. The controller performance under the change of load disturbance, is better for the case I with sampling frequency of 100 kHz, however, Case III with sampling frequency of 50 kHz is comparable to it.

Furthermore, the effect of the sampling time on speed controller and THD is also studied and investigated. The performance of speed controller is slightly better for higher sampling frequency. Furthermore, the current ripple calculated in the form of THD is lower corresponding to higher sampling frequency. As the sampling frequency increases, the difference between the errors for consecutive samples reduces that ultimately reduces the current ripples. Therefore, reduction in current ripple is achievable for even lower

switching frequency with higher sampling frequency operation. The sampling frequency and the time synchronization both have the impact on motor performance. An appropriate synchronization methodology and sampling time can achieve the better performance in terms of transient response under change in reference speed and motor load.

Chapter 4

MODERN PMSM DRIVE: FINITE SET MODEL PREDICTIVE CONTROL

4.1 Introduction

Several control strategy has been used for the control of the motor. Among these controls the conventional field oriented control (FOC), direct torque control (DTC) are widely used for the industrial applications. The FOC has a good steady state performance as compared to that of the DTC. Moreover due to the absence of the hysteresis band the digital implementation of the FOC is easier. However the FOC utilizes cascaded PI controller for its implementation which leads to the sluggish response of the system. More over the tuning of the PI is a tedious work to perform.

Due to the good dynamics and flexibility for inclusion of nonlinearities and multiple constraints the model predictive control (MPC) are recently getting attraction among the researcher. The MPC can be broadly classified in to two category as continuous set model predictive control (CS-MPC) and Finite set model predictive control (FS-MPC). The CS-MPC uses the continuous voltage vector through a modulator for the generation of the switching signal. Whereas the FS-MPC considers only a finite set of possible switching states of the power converter for the generation of the gate signals. The main advantage with the FS-MPC is that it can generate the switching signal directly by optimizing the control parameters.

4.2 FS-MPC Working Principle

FS-MPC is one of the most trendy control schemes of the wide family of model predictive control. It is characterized by the use of a discrete-time model of the system to predict the future behavior of the variables to be controlled based on the possible switching

states of the power converter. The FS-MPC does not require a cascaded structure of the control loop and does not need a modulator to generate switching signals of the power switches.

The system is considered as a finite set of linear discrete-time models corresponding to the finite switching states. These models are used for the prediction of the future behavior of controlled variables for each switching state to determine the optimum actuation in each sampling interval to achieve the control objectives. The control objectives are governed by a predefined objective function or cost function that is formulated considering controlled variables and desired references. The optimum actuation is selected according to the minimum cost function in each sampling interval and directly applied to the power converter.

The block diagram of a general FS-MPC scheme applied to power converters and drives is depicted in Fig. 4.1. The power converter shown in the figure can be of any one of the power converter topologies and any number of phases. The generic load in the figure can be represented by any form of electrical load such as passive load, active load, electrical

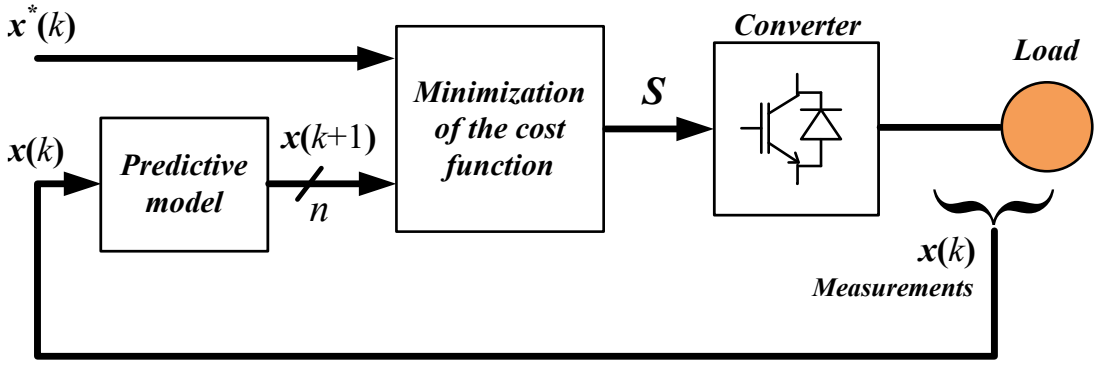


Fig. 4. 1. General block diagram of the FS-MPC scheme for power converters.

machine, and the grid. In the FS-MPC scheme, a sampled form of measured variables $x(k)$ is used in the model to calculate predicted controlled variables $x(k+1)$ for each one of the n possible actuations, that is, switching states, voltages, or currents. After the completion of the prediction step, the values of the corresponding cost functions are evaluated with

respect to the error between the predicted $x(k+1)$ and reference values $x^*(k)$. Finally, the optimum actuation S is selected corresponding to the minimum cost function and applied to the converter.

4.3 FS-MPC for PMSM drive

The FS-MPC utilizes the discrete-time model of the system and the possible switching states of the three-phase voltage source inverter for the execution of the control algorithm. Total number of the switching states corresponding to the three-phase VSI are eight and corresponding to these eight switching states, eight voltage vector can be obtained as given in the Table 4.1. For every possible states of the power devices of the converter, the controller predicts the future behavior of the system variables for the next sampling time. The controller evaluates the values of cost functions based on these predicted variables of the system. Finally, corresponding to the minimum cost function, the switching signal is generated for the power devices in each sampling time. The implementation of the FS-MPC for the PMSM drive is illustrated in the Fig.4.2. The control implementation can be divided in to two part as follows:

Table 4.1 Voltage vectors of three phase VSI

Switching state $[S_a, S_b, S_c]$	**Voltage Vectors** $[V_\alpha, V_\beta]$	**Vector Number**
[0,0,0]	[0,0]	0
[1,0,0]	$[2V_{dc}/3,0]$	1
[1,1,0]	$[V_{dc}/3, \sqrt{3}V_{dc}/3]$	2
[0,1,0]	$[-V_{dc}/3, \sqrt{3}V_{dc}/3]$	3
[0,1,1]	$[-2V_{dc}/3,0]$	4
[0,0,1]	$[-V_{dc}/3, -\sqrt{3}V_{dc}/3]$	5
[1,0,1]	$[V_{dc}/3, -\sqrt{3}V_{dc}/3]$	6
[1,1,1]	[0,0]	7

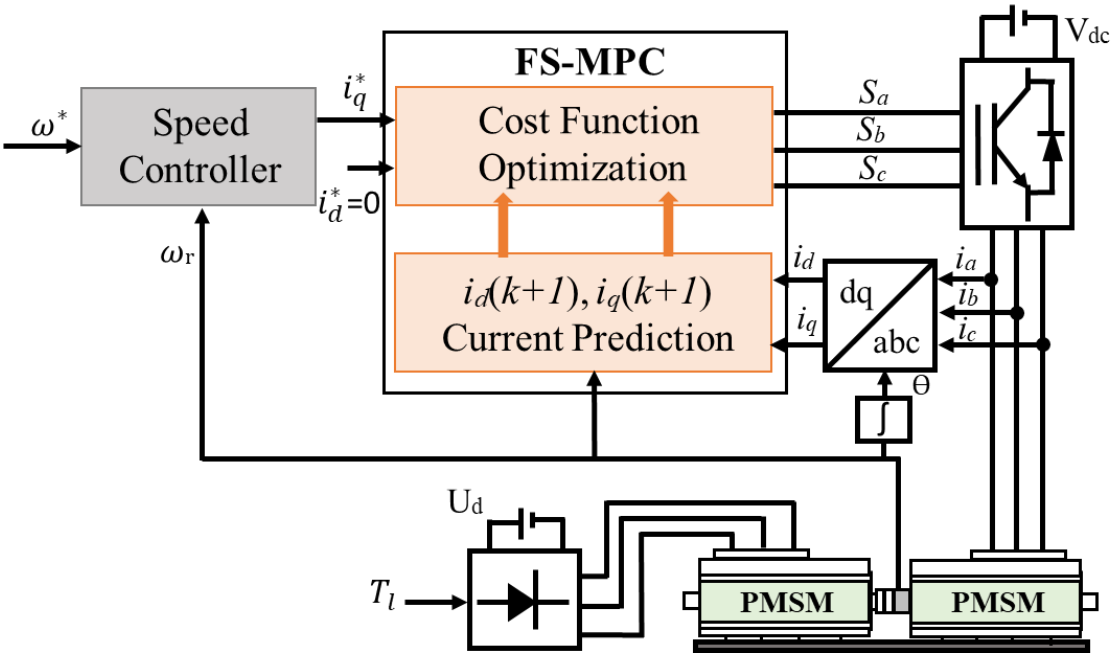


Fig.4.2. Schematic diagram of FS-MPC based PMSM Drive

4.3.1 Discrete time predictive model

In this work, the discrete model of the PMSM is considered as a prediction model for the system implementation. The discrete time model is used to predict the future behavior of the motor current from the supply voltage and the measured current at the instant of *k*. As already discussed in the previous chapter, the forward Euler discretization method is used to approximate the discrete-time load current derivative *di/dt* for a sampling time T_s , which is given as:

$$\frac{di}{dt} \approx \frac{i(k+1)-i(k)}{T_S} \tag{4.1}$$

The discretized motor current on *dq* axis is obtained by applying the relation of equation 4.1 in the continuous time equation as presented in the following equations:

$$i_d(k+1) = K_1 i_d(k) + K_2 \omega_r(k) i_q(k) + K_3 v_d(k) \tag{4.2}$$

$$i_q(k+1) = K_1 i_q(k) - K_2 \omega_r(k) i_d(k) + K_3 v_q(k) - K_4 \omega_r(k) \tag{4.3}$$

Where, $K_1 = (1 - R_s T_s / L_s)$, $K_2 = T_s$, $K_3 = T_s / L_s$, $K_4 = \psi_m T_s / L_s$. $i_d(k+1)$ and $i_q(k+1)$ are the motor predicted current at the instant of $k+1$. Based on the present sampling current $i(k)$, speed $\omega_e(k)$ and the given stator voltage $v(k)$, the prediction current is evaluated for the next sampling instant $(k+1)$. These equations predict the stator current for each one of the voltage vector of the eight voltage vector of the inverter.

4.3.2 Evaluation of Cost Function

The cost function can be expressed as the error between the reference current and the predicted current:

$$G = (i_d^* - i_d^j(k+1))^2 + (i_q^* - i_q^j(k+1))^2 \quad j = 0,1,.....7 \tag{4.4}$$

Where id^* and iq^* are the reference stator current on the d and q axis respectively and $\boldsymbol{i_d^j}$ $(k+1)$ and $\boldsymbol{i_q^j}$ $(k+1)$ are the predicted current corresponding to the inverter voltage vector and j represents the number of predicted current according to the number of possible switching states. The i_d^* is considered to be zero in case of the SPMSM. The first term of the cost function represent the minimization of the reactive power. The second term is use to track the torque producing current.

4.4. XSG based Controller Designing

The controller development of the motor drive system consist of two part: speed controller and the FS-MPC. The implementation of FS-MPC consists of three steps: prediction of the motor current, evaluation of cost function, and generation of switching signal corresponding to the optimized cost function. The digital designing tool XSG integrated with the MATLAB/Simulink is used for the designing of the controller that ultimately used for the FPGA based system development.

4.4.1 Speed Controller

The controller implantation require reference value corresponding to the desired operation. The speed controller loop consists of a PI controller to regulate the motor speed and correspondingly generates the reference quadrature axis current i_q^* . The implementation of the speed controller in XSG is presented in the Fig.4.3. The XSG based FPGA implementation requires the discretization of the PI controller. Euler's forward method is used for the discretization of the controller. The discretized equation for the PI control is presented as:

$$i_q^*(k) = K_{p\omega}\omega_{er}(k) + x_\omega(k)$$
$$x_\omega(k) = x_\omega(k-1) + K_{i\omega}T_s\omega_{er}(k) \quad (4.5)$$

Where $i_q^*(k)$ and $\omega_{er}(k)$ are the reference q axis stator current and speed error at the instant k. $x_\omega(k)$ is the output of the integral control at the instant k. For the FS-MPC designed in dq reference model, three-phase sensed motor current need to be converted into their equivalent dq axis current.

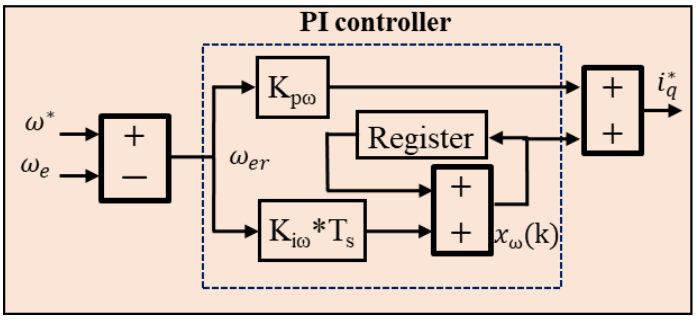


Fig.4.3. XSG based design of speed control loop

4.4.2. Prediction Model

The discrete-time mathematical equations described in Section 4.3 is used for the prediction of the motor current. The cost function is computed using an absolute error

between the reference current and the predicted current. For the implementation of FS-MPC in *dq* frame, the evaluation of the cost function corresponding to a voltage vector *j* is shown in Fig.4.4. The cost function G_j can be evaluated for the voltage vectors *j*. For a two level inverter, there are eight voltage vectors and hence corresponding to eight voltage vector there will be eight cost functions.

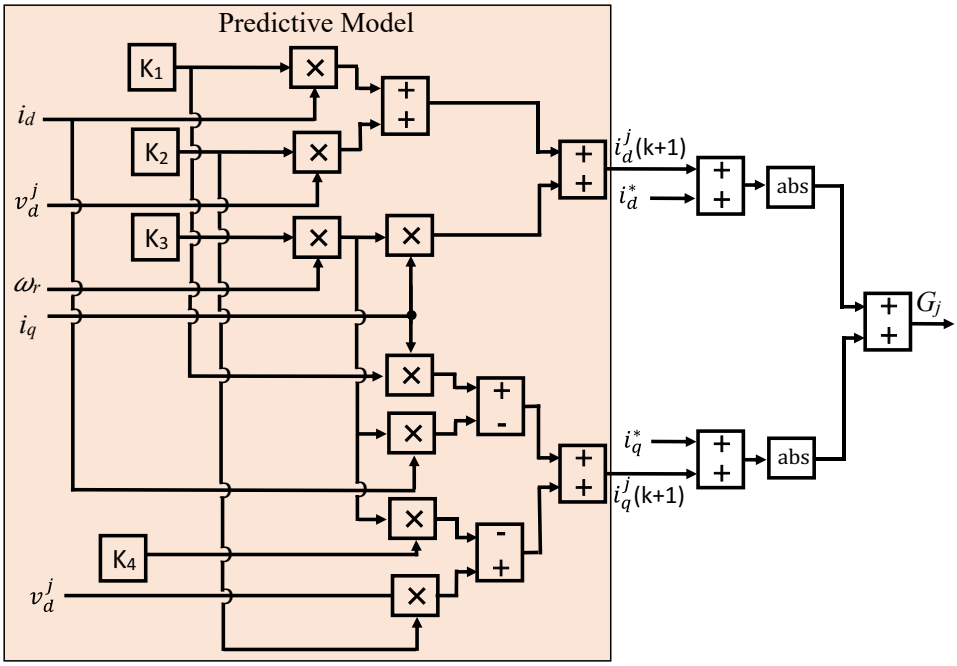


Fig.4.4. XSG based design of current prediction and cost function

4.4.3 Cost Function Optimization and selection of switching vector

The block diagram representing the cost function optimization G_{opt} and selection of an optimum switching state S_{opt} is shown in the Fig.4.5. In order to compute the optimized cost function, a pipelining method is used. The cost functions are connected to one another to form a pipe like structure. The two consecutive cost functions in the pipe line structure are compared by a comparator (C) and the minimum among these is selected through a 2:1 multiplexer (M). The output of the comparators (binary digit "0" or "1") are used as select lines (sel_1–sel_7) for the multiplexers. These combinations of the comparator and Mux (C&M1-C&M7) is used for all the possible cost functions (G_1-G_8) to select the optimized

cost function G_{opt}. The switching signal (S_1-S_8) corresponding to the voltage vector (V_1-V_8) are used in a pipe line structure to find the optimized switching signal. The select lines (sel_1–sel_7) is used for a 2:1 mux to find the optimized switching signals S_{opt} as shown in the Fig. 4.5. Finally the optimum switching signal is sliced to switching signal S_a, S_b, S_c. The Inverter used for the experimental validation has inbuilt inversion circuit with dead time compensation for the PWM signal. Therefore, the switching signals are only generated for the upper half power devices of the inverter.

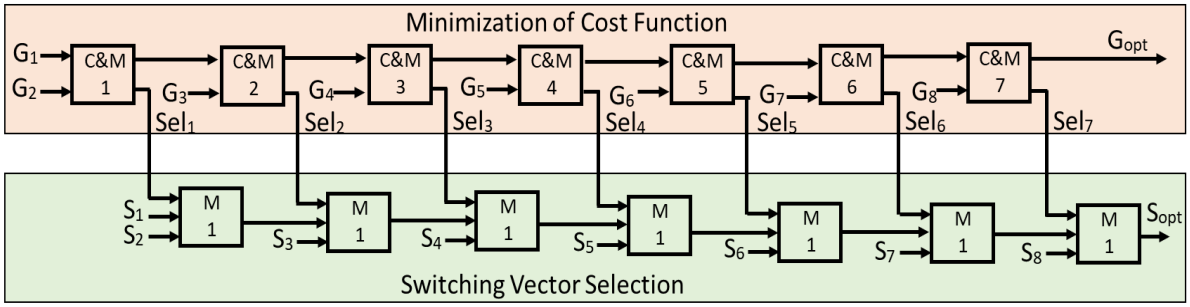


Fig.4.5. Cost function minimization and switching vector selection

4.5. FPGA based system Implementation

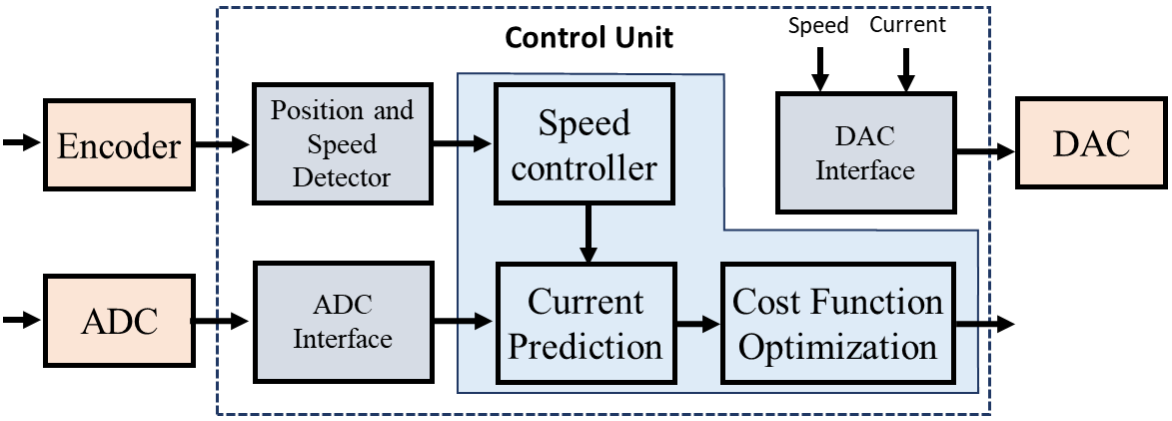


Fig.4.6. FPGA based system implementation.

The FS-MPC based PMSM drive system in Fig.4.6 is designed and developed using the digital control environment of FPGA. The control requires the sensed motor current

and speed for its implementation in FPGA. The three phase motor current is sensed through a current sensor and passed through a level shifter. The shifted value of the measured current is fed to the FPGA by using an analog to digital convert (ADC). The digitized data from the ADC are synchronized at the rate of sampling frequency through ADC interface unit. The encoder is used to sense the motor position and motor angular speed as a pulse with resolution of 2048 pulses per revolution. The motor speed and positions can obtained from this unit by using the position and speed detector .Finally this parameter are fed to the control unit for the generation of the switching signal. For monitoring and validation the digital signal are converted to analog signal by using a digital to analog converter (DAC). The control unit along with the position and speed detector, ADC, (DAC) interface unit is programmed to the FPGA board.

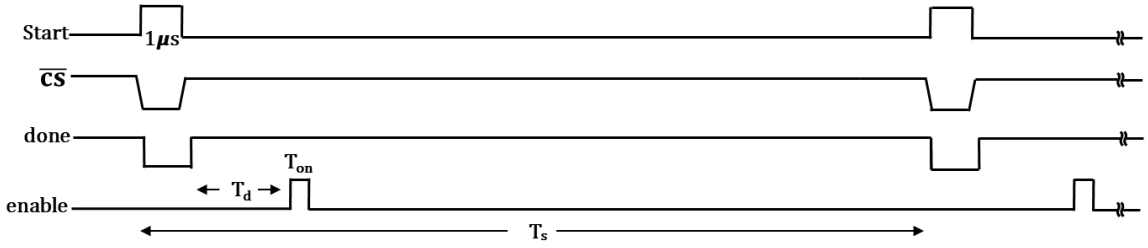


Fig.4.7. Timing diagram of the control loop

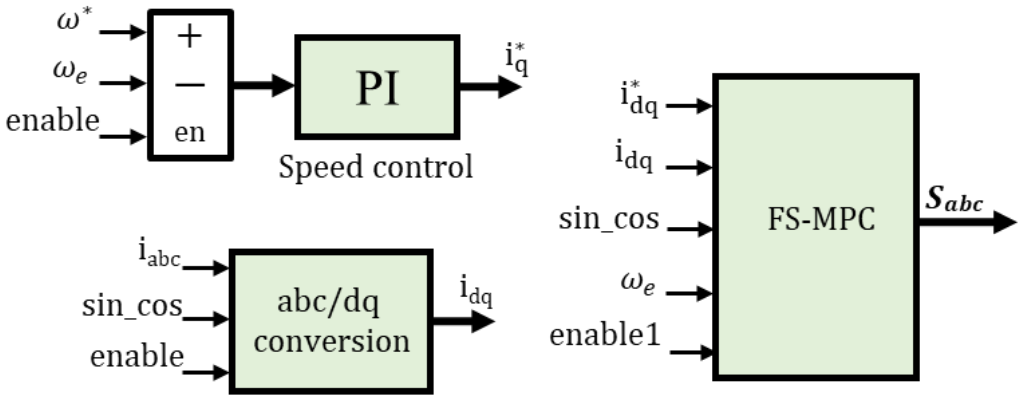


Fig.4.8. Controller implementation in FPGA

For the implementation of control unit, the output of speed control unit is responsible for the motor current prediction, therefore a sequential time synchronization is used within a

sampling time. The timing diagram used for FPGA implementation is shown in the Fig.4.7. The start signal has on time of 1μs and its width is defined by sampling time T_s. Consequently, the chip select and the done signal was switched to a high state and the start signal switched to the low state after completion of the conversion of the analog signal to the digital signal by the ADC interface unit. The enable signal is generated with on time of T_{on} and delay time of T_d. The done signal in Fig. 4.7 as an enable signal enables the speed controller loop as well as abc to dq conversion simultaneously to perform parallel computation. The output of the speed control unit (i_q^*) and abc to dq conversion (i_{dq}) is fed to the FS-MPC unit for implementation of the control algorithm. Further the enable1 signal with on time T_{on} of 0.5μs and with delay time T_d of 1.5 μs from the enable signal enables the FS-MPC unit as shown in the Fig.4.8.

4.6. Experimental Results and Discussion

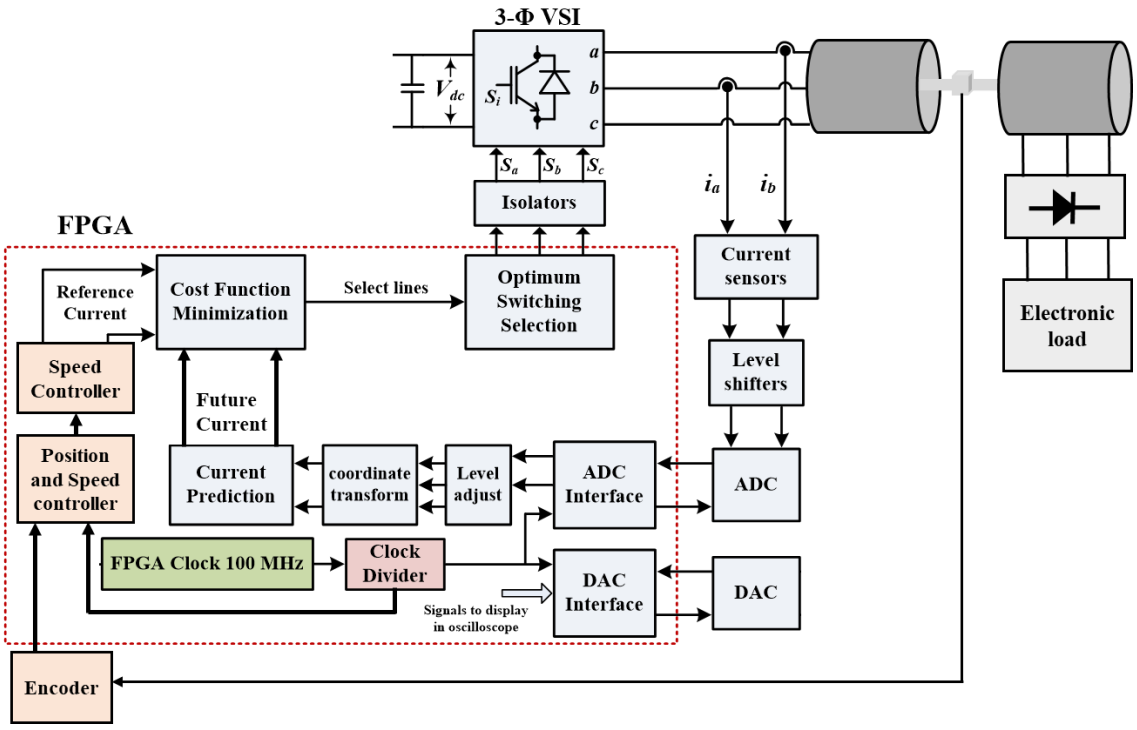


Fig.4.9. Experimental prototype for FS-MPC based PMSM drive system

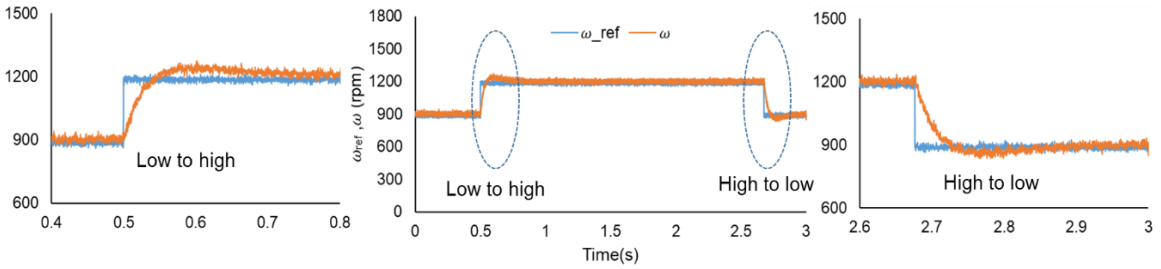
An experimental setup as illustrated in the Fig.4.8. is developed for the real time implementation and analysis of the FS-MPC for FPGA based PMSM Drive System. The FPGA code was generated automatically through the modelled controller and programmed using dedicated software (Xilinx VIVADO Design Suite) for real-time operation of FS-MPC. Sampling frequencies of 25 kHz, 50 kHz and 100 kHz are used for the extensive analysis of impacts of the sampling frequency on the motor performance. A step change in speed reference and motor load condition (load disturbance) is introduced to demonstrate the system performance (current and speed) under transient and examine corresponding to different sampling frequencies. Moreover, the motor current harmonics distortion corresponding to different sampling time is also considered to demonstrate the system performance. The system parameters and the component specifications consider for the development of the experimental setup are explained in the Table 4.2 and 4.3. For the FPGA based system implementation a clock frequency of 100 MHz is consider.

4.6.1. Change in Reference Speed

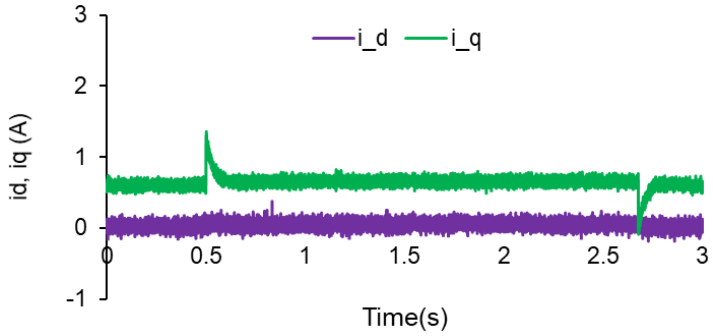
Depending upon the applications, the motor may undergo change in reference speed. The controller should attain the new reference smoothly with lower settling time. A step change in the reference speed from 900 rpm to 1200 rpm (low to high speed) and 1200 rpm to 900 rpm (high to low speed) is considered to demonstrate and analyze the performance of the controller for the PMSM drive system.

The Fig.4.10, Fig.4.11 and Fig.4.12 demonstrates the speed regulation of PMSM for the sampling frequency of 25 kHz, 50 kHz and 100 kHz respectively. The response is expanded from 0.4s to 0.8s and 2.6s to 3s for a close view of the speed dynamic response for change in reference speed from low to high and high to low respectively. The settling time performance of speed regulation is better for 100 kHz and 50 kHz as compared to 25 kHz. With increase in the sampling frequency the error between the reference and the predicted current decreases, that ultimately improves the dynamic performance of the speed response. Further, the motor current i_d and i_q are shown corresponding to the sampling times. The i_q for the sampling frequency of 100k shows better transient performance. With increase of the sampling frequency the controller shows better transient

performance. The settling time performance of speed regulation is summarized in Table 4.2 in terms of time required to attain the steady state.

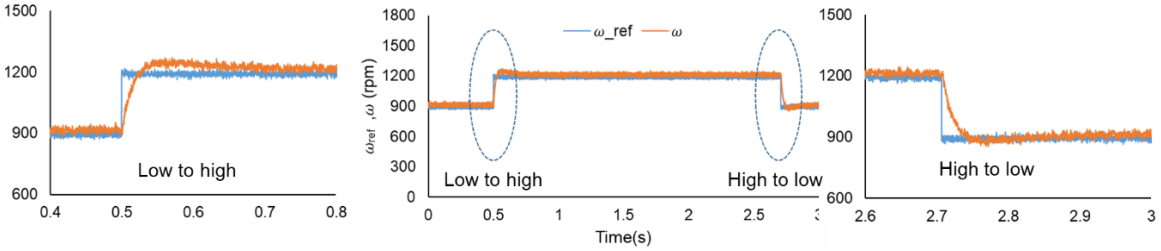


(a)

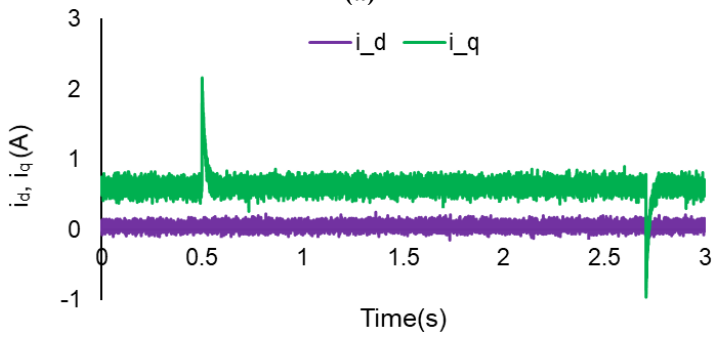


(b)

Fig.4.10. (a) Motor speed response (b) current response for sampling frequency of 25 kHz

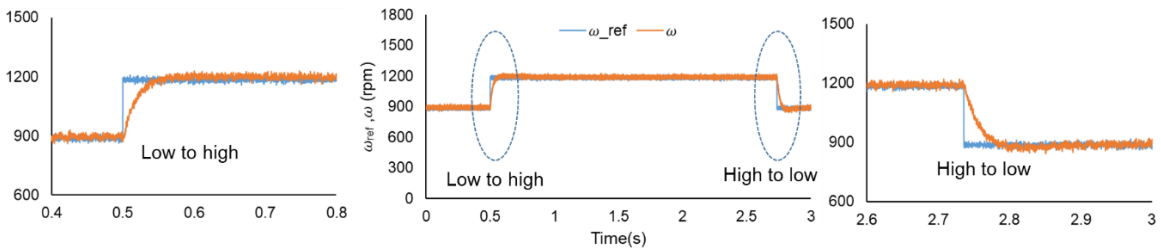


(a)



(b)

Fig.4.11. (a) Motor speed response (b) current response for sampling frequency of 50 kHz



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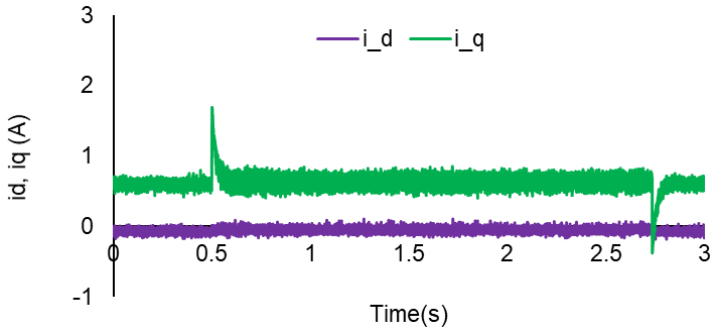


(b)

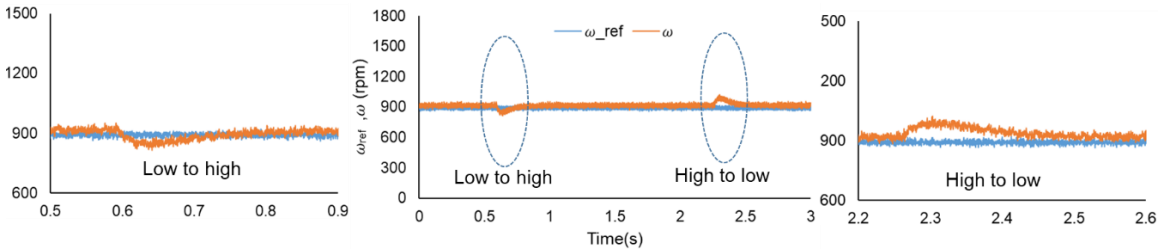
Fig.4.12. (a) Motor speed response (b) current response for sampling frequency of 100 kHz

Table 4.2. Speed response corresponding to the change of reference speed

Sampling frequency (kHz)	Low-high	High-low
25	0.3s	0.08s
50	0.2s	0.05s
100	0.05s	0.025s

4.6.2. Change in Load Condition

The motor system can go under the load disturbance condition as well and the transient performance of motor drive system is of concern to attain the desired reference speed smoothly with lower settling time. A step change in the electronic load to introduce a load disturbance is employed that ultimately results in motor current change from 0.5A to 1A (low to high) and 1A to 0.5A (high to low). The motor speed is kept to 900 rpm for all the operating conditions.



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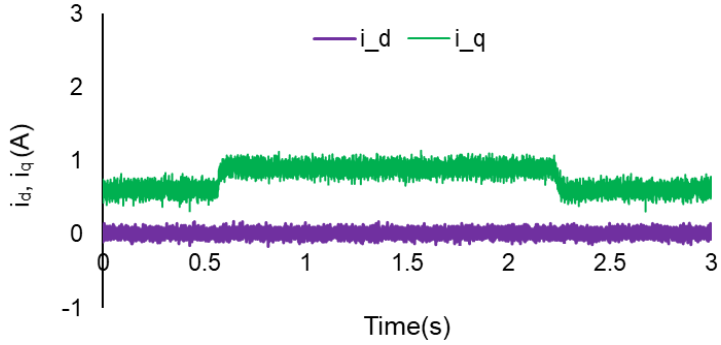
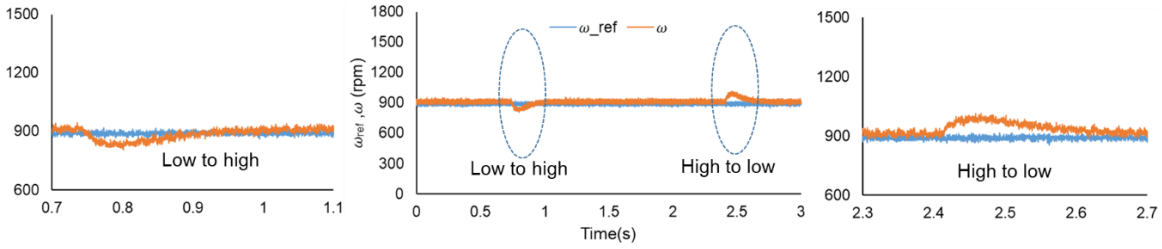
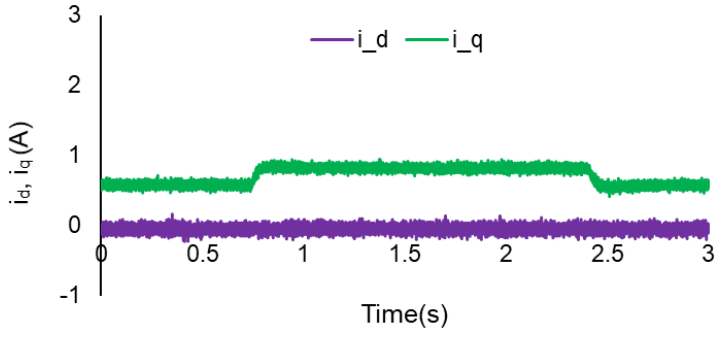


(b)

Fig.4.13. (a) Motor speed response (b) current response for sampling frequency of 25 kHz

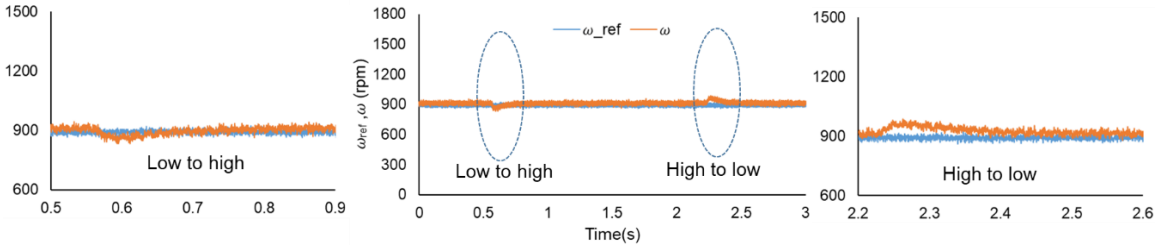


(a)

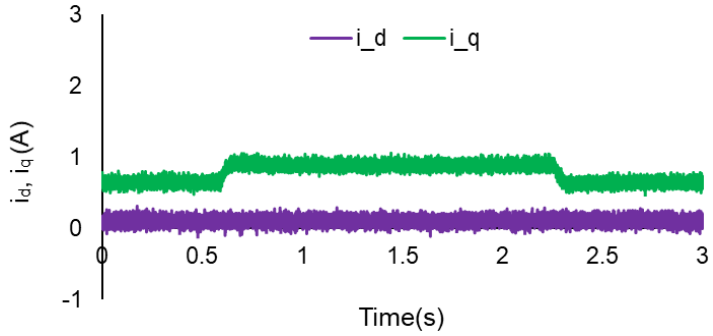


(b)

Fig.4.14. (a) Motor speed response (b) current response for sampling frequency of 50 kHz



(a)



(b)

Fig.4.15. (a) Motor speed response (b) current response for sampling frequency of 100 kHz

The speed regulation of PMSM under load disturbance in Fig.4.13, Fig.4.14 and Fig.4.15 is demonstrated for the sampling frequency of 25 kHz, 50 kHz and 100 kHz. The response is expanded for 4s for a close view of the speed dynamic response for change in load disturbance from low to high and high to low respectively. The settling time performance of 100 kHz sampling frequency is showing better performance for both high to low load and low to high load. The settling time performance of speed under load disturbance is summarized in Table 4.3 considering the time required to attain the steady state.

Table 4.3. Speed response corresponding to the change of load

Sampling frequency (kHz)	Low-high	High-low
25	0.15s	0.26s
50	0.18s	0.24s
100	0.04s	0.17s

4.6.3. System Performance in Terms of THD

The controller performance (three phase current harmonics) depends up on the switching frequency at which the power devices are operating. In case of the FS-MPC the switching frequency of the power devices is governed by the sampling frequency. Therefore, different sampling frequencies are considered to examine and analyze the controller performance. The maximum switching frequency of the FS-MPC is half to the sampling frequency consider for the system implementation. The maximum switching frequency that can be taken for the inverter use for the experimental system is 50 kHz. Considering this condition maximum sampling frequency of 100 kHz can be used for the system implementation. Different sampling frequency are exercised to investigate the system performance as shown in the Table 4.4. For all the cases the motor is operated at a speed of 900 rpm and current of 0.7A for low load case and 1.2 A for the high load case.

Under higher harmonic conditions the motor have more iron losses which ultimately reduces the motor efficiency and service life. Moreover, with increase in the harmonics the motor can have noise and vibration. As the switching frequency increases the harmonics in the current decreases. Therefore, for better performance the controller should work at higher switching frequency that means higher sampling frequency in case of the FS-MPC. However, with increase in the switching frequency the switching losses increases which ultimately increase the size of the converter. According to the IEEE standard the current THD of less than 5 percent is acceptable. Therefore by considering both the system performance and the losses the sampling frequency of 50 kHz can be a better option.

Table 4.4. The THD comparison

Sampling Frequency (kHz)	% THD for Low load	%THD for high load
10	12.6	8.02
25	6.2	4.1
50	3.7	2.4
100	2.3	1.3

4.6.4. Steady State Error Analysis

In order to analyze the accuracy of the controller, the steady state error (SSE) of the motor current is considered. The comparative analysis of the SSE is performed corresponding to different sampling frequencies through bar graphs. The SSE is calculated by using the bellow equations:

$$\text{SSE} = \frac{\sqrt{\bar{e}_d^2 + \bar{e}_q^2}}{\sqrt{i_d^* + i_q^*}} \times 100 \tag{4.6}$$

$\bar{e}_d$ and $\bar{e}_q$ are the mean value of the dq axis current error. These error can be calculated as follows:

$$\bar{e}_d = \frac{1}{N}\sum_i \left\{ i_d^*(j) - i_d(j) \right\} \tag{4.7}$$

$$\bar{e}_q = \frac{1}{N}\sum_i \left\{ i_q^*(j) - i_q(j) \right\} \tag{4.8}$$

Where N is the number of the current samples considered for the calculation of the SSE.

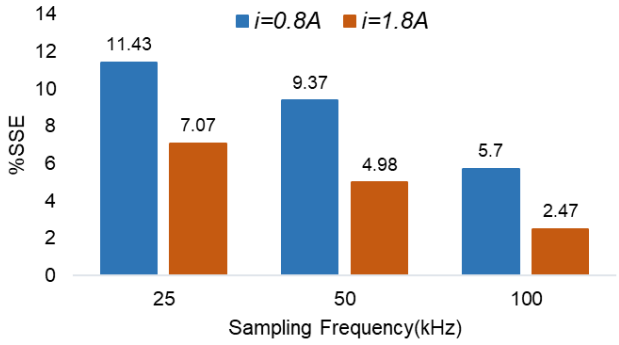


Fig.4.16. SSE for FS-MPC

The SSE comparison for the sampling frequency of 25 kHz, 50 kHz and 100 kHz is shown in the fig. 4.16. The motor is working at speed of 900rpm. The motor current of 0.8 A and 1.8 A is considered for the calculation of the steady state current. The steady state error decreases with the increase of the sampling frequency and motor current.

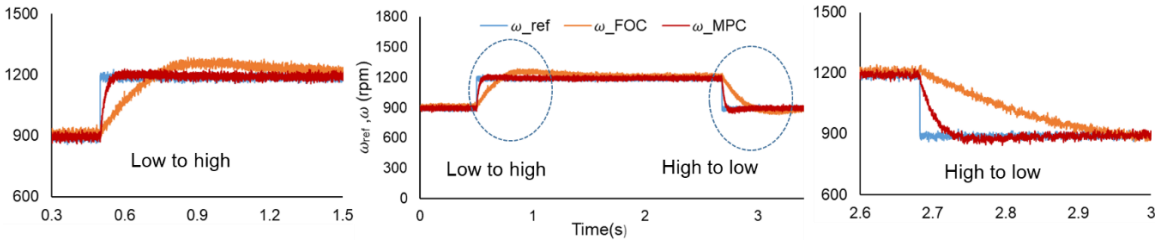
4.6.5. Comparison with FOC

In order to validate the system behavior of FS-MPC the dynamic speed response is compared to that of the linear control FOC. The sampling frequency for both the controller is kept same that is 100 kHz. The speed controller gain $K_{p\omega}$ and $K_{i\omega}$ is considered to be same. The values of the controller gain (speed control and current control) is illustrated in the Table 4.5.

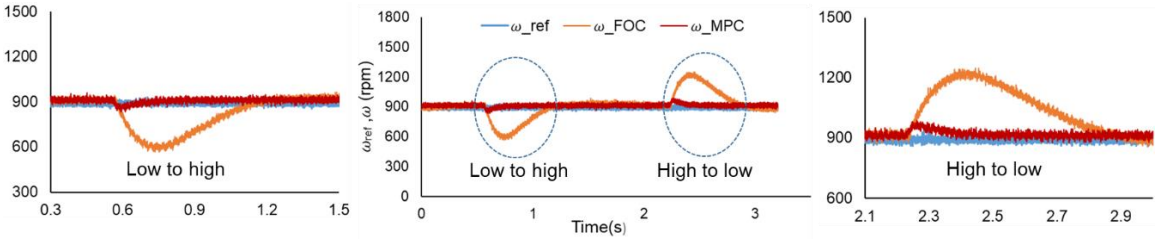
Table 4.5. Controller parameter

Parameter	Value
$K_{p\omega}$	3
$K_{i\omega}$	30
K_{pd} , K_{pq}	5
K_{id} , K_{iq}	20

The comparative regulatory behavior of speed control for the change in speed from 900 rpm to 1200 rpm is illustrated in the Fig. 4.17.a for sampling frequency of 100 kHz. In case of FOC the overshoot for the speed change is higher as compared as that of the FS-MPC. Moreover the settling time is also more as compared to that of the FS-MPC. Similarly the speed response corresponding to the change in load disturbance is also illustrated in the Fig.17.b. The speed response in case of FOC has slower response as compared to that of the FS-MPC. Moreover, the speed undershoot and overshoot is more than twice as compared to that of FS-MPC. Further the detail comparison of the two controller are presented in the Table 4.6.



(a)



(b)

Fig.4.16. Motor speed response for sampling frequency of 100 kHz (a) change in speed reference (b) change in load condition

Table 4.6. Controller Comparison

	FOC	FS-MPC
Speed Controller	PI	PI
Inner Controller	2 PI	Cost Function
Tuned Parameter number	6	2
pulse width modulation	yes	no
switching frequency	constant	variable
Computational burden	Low	High
Inclusion of System constraints	Difficult	easy

4.6.6. Stability analysis of the FS-MPC

The optimization cost function, in this FS-MPC is as follows:

$$G = (i_d^* - i_d^j(k+1))^2 + (i_q^* - i_q^j(k+1))^2 \qquad (4.9)$$
$$j = 0,1,.....7$$

Equation 4.9 clearly describes the cost function has a convex optimization problem. Hence it has only one local minimum which can act as global solution. To converge towards this global solution, the switching states will be decided at each fs =25 kHz (for the case of lowest sampling frequency). This switching decision making time is fall little than inertia time constant Tj (Tj=5.1s) of the motor. Hence current controller implemented in present FS-MPC scheme is always converges to the reference current (synthesized by the speed controller) value by minimizing cost function given equation 4.9. So by

neglecting the current controller time constant, the open loop gain of the proposed closed loop is given as follows.

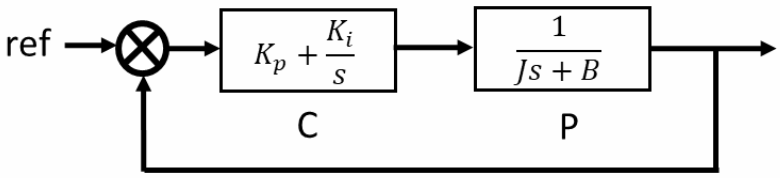


Fig. 4.17. Closed loop speed controller

The open loop gain (O.L.G) of above closed loop speed controller is as follows

$$\text{O.L.G (s)} = \text{C(s)*P(s)} = \frac{196078.43s + 1960784.3}{s^2 + 0.65s} \quad (4.10)$$

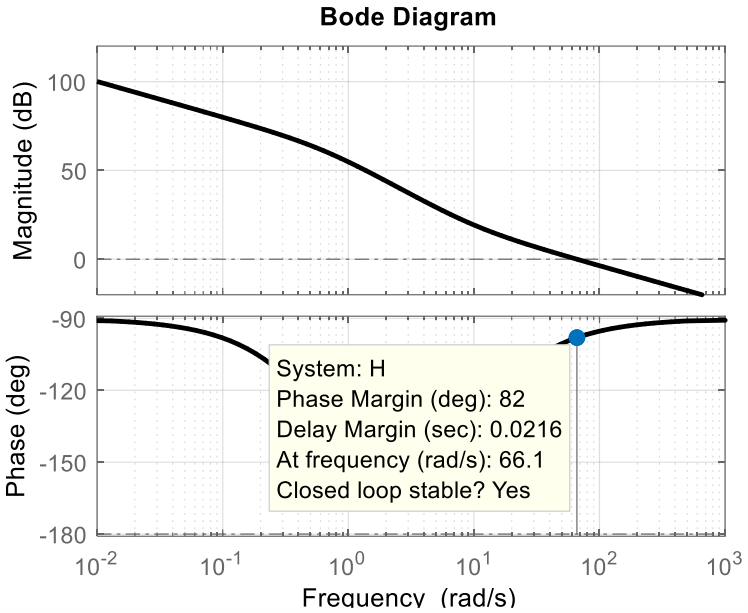


Fig. 4.19. Bode diagram of the PMSM drive system

As from the above Fig.4.19 the phase margin and the gain margin is positive the system is stable. As we said before the current controller has negligible impact on the settling time as the bandwidth of the current controller is far greater than the speed controller.

4.7 Summery

Finite set model predictive control (FS-MPC) has been inducted for motor drive system. The dynamic response, multiple constraints handling nature of FS-MPC are the major factors that stands out amongst the controller family. However, for real time implementation, the computational burden of the FS-MPC is a primary concern. Due to the parallel processing nature and discrete nature of the hardware platform, the field programmable gate array (FPGA) can be an alternative solution for real-time implementation of the controller algorithm. Nevertheless, FPGA is capable of handling the computational requirements for the FS-MPC implementation, however, the system development involves multiple steps that lead to the time-consuming debugging process. Moreover, specific hardware coding skill makes it more complex corresponding to an increase in system complexity that leads to a tedious task for system development.

This chapter, presents FPGA based real time implementation of FS-MPC for PMSM drive system. The FS-MPC algorithm is developed for a three phase two level voltage source inverter (VSI) fed PMSM drive system using an optimization function in terms of current. Step by Step design and development of the controller for the motor drive system is explained. The motor dynamics response is analyzed corresponding to different sampling frequency. Moreover, the harmonics in the motor current is also consider corresponding to different sampling frequencies. To analyze the dynamic behavior of the motor, a step change in the speed reference and load disturbance is introduced. Furthermore, a model based approach has been adopted for the system implementation for the modelling of the FS-MPC. For the real time implementation on FPGA, the controller is developed in XSG environment integrated with the MATLAB/Simulink that automatically generate the HDL code.

The sampling frequencies have a significant impact on motor performance under transient operation. The controller demonstrates better performance for sampling frequency of 100 kHz under change of speed reference and also change of the load condition. Furthermore, the effect of the sampling frequency on THD is also studied and

investigated. The current ripple calculated in the form of THD is lower corresponding to higher sampling frequency. As the sampling frequency increases, the switching frequency increases that ultimately reduces the current ripples. The sampling frequency have the impact on motor performance, with increase of sampling frequency the controller can achieve a better performance in terms of transient response under change in reference speed and motor load condition. In addition, the controller performance is also compared to the FOC PI-PI controller. A faster response for FS-MPC is obtained compared to that of the FOC that ultimately validate the proposed method.

Chapter 5

ADVANCE PMSM DRIVE, HYBRID CONTROL: 2DoF-FSMPC, DAHCC-FSMPC

5.1 Introduction

Due to the high dynamic response, multiple variable control and flexible nature the model predictive control (MPC) techniques are getting attentions among the power electronics and drives researcher. According to the switching control technique, the MPC can be categorized as continuous control set MPC (CS-MPC) and finite control set MPC (FS-MPC). In the CS-MPC approach, for the generation of switching signals modulator is necessary, moreover it associated with complex algorithm and implementation. However in second strategy the switching signals can be generated directly by using the finite number of switching states. Moreover it has ability to add various constraints for better dynamic response of the system at target conditions. Due to the easy implementations of FS-MPC it has a wide range of application such as in the VSI fed motor drive system, traction and servo drives, and wind turbine power generation also in grid connected systems. The speed regulation of motor system is imperative in the motor drive control. During the operation, the motor may undergo different kind of disturbance due to the change in load condition as well as change in reference speed depending on operating conditions. Due to the simple design and implementation, the conventional PI control is widely use to realize the speed regulation of the motor.

The speed regulation in conjunction with inner current control loop governs the performance of the motor drive system. In the inner current control loop the FS-MPC is employed to improve the dynamic performance corresponding to change in operating condition of the motor drive system. However, the controller for speed regulation under

achieve the performance due to limitation of conventional PI control that will ultimately impact the overall dynamic performance of the system.

The requirements to improve the dynamic performance under transient condition occurred due to an alteration in operating condition, is to reduce the settling time. Moreover, reduction in settling time can results in higher overshoot/undershoot during the transients. The fast dynamic response corresponding to the reference speed and a robustness to the load disturbance is always desirable through the speed controller design. Therefore, to obtain a better trade-off and optimized performance a sub-control is necessary that can be realized by incorporating additional controller gain along with conventional controller. This is defined as the degree of freedom of the controller.

This work presents a two-degree-of-freedom (2-DoF) control strategy to enhance the dynamic performance of motor speed regulation. The 2-DoF control design is consisting of a conventional PI controller and an additional proportional gain as a feedforward loop.

In addition to many advantages the FS-MPC has some drawback. The main drawback with this technique is variable switching frequency which ultimately leads to increase in switching losses, spread switching frequency spectrum and poor system performances. The switching harmonic spectrum depends on the commutations of the converter's power switches, which in FS-MPC is not guaranteed to occur at the fixed sampling frequency. Due to the variable switching frequency the filter design and the thermal design became more difficult which leads to the increase of the overall cost of the system.

To make the switching frequency constant many attempts were made in the past for different applications such as in grid connected system, motor drive system and multilevel inverter with RL load. The predictive control with discrete space vector modulation (DSVM) in [80] was implemented for the power converter. The main advantage with this approach is it gives good performance at the low sampling frequency, while the computational burden increases to achieve the objectives. A modified DSVM with FS-MPC [81] is proposed for the RL load to achieve constant switching frequency. In this paper, the author is able to reduce the common mode voltage with this technique, while the

number of calculations increases. In [82] a modulated model predictive control was proposed for both the RL load and PMSM in the over modulation region. This method gives a fast dynamic response compared to the basic FS-MPC. However, the setting of the current at the reference signal gives a dip in the amplitude. The basic FS-MPC combined with a modulator in [83] was implemented for the PMSM drive. In order to make the switching frequency constant, the voltage vectors are dynamically selected and calculated by an optimization algorithm. However, this method involves a large number of calculations for the evaluation of the suitable voltage vector which leads to an increase in the system complexity and computational burden.

In this work a novel control is proposed which allow the controller to work at predefined frequency. The FS-MPC as a current controller generates the switching signal based upon the selection of the voltage vector corresponding to the optimized current error. Similarly, HCC generates the switching signal based on the current error passed through the hysteresis band. For both the cases, the main concern is the variable switching frequency. To overcome this drawback in HCC, it is combined with the modulation techniques, like that of the FS-MPC case. Moreover, an adaptive hysteresis band method is also used with conventional HCC to make the switching frequency constant. The optimized minimum error obtained from the FS-MPC can be used to generate switching signals by passing through the discrete adaptive band HCC (DAHCC).

5.2 2-DoF based FS-MPC

The speed control is uses the speed error to generate the reference current for the control of the motor. The error signal is represented as:

$$\omega_{er}(k) = \omega_r(k) - \omega_e(k) \tag{5.1}$$

The error signal can be processed through the PI control or the 2 DoF control for the evaluation of the reference signal.

5.2.1 Conventional PI Control

The conventional PI controller has been utilize for the speed regulation of the motor. The simple diagram representing the PI control is shown in the Fig.5.1. The limitations of the PI control is that the system has just one freedom to achieve the control speed of the motor. By tuning the proportional and integral gain of the PI control we may achieve the desire response. However with change of the reference and the load disturbance the system may not able to get good transient response.

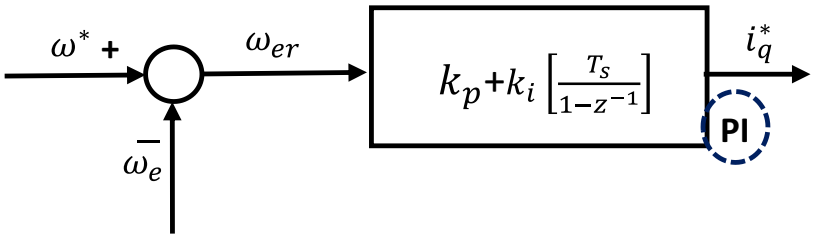


Fig.5.1. Conventional PI control

5.2.2 2-DoF PI Control

The 2-DoF speed controller has advantage of having extra degree of freedom for the controller tuning as compared to the PI controller. Therefore the transient response of the system may improve by using the 2 DoF method. There are several structure of the 2 DoF controller which can be adopted for the speed regulation. In this work a simple PIP based 2 DoF control is use for the regulation of the speed control as shown in the Fig.5.2.The 2 DoF uses an extra proportional gain in addition to the PI control to minimizes the speed error.

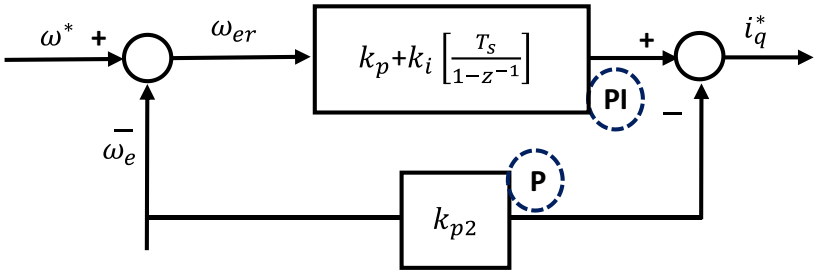


Fig.5.2. 2 DoF PIP control

5.2.3 Modelling of 2DOF speed controller

The 2 DoF based speed controller by is represented in the Fig.5.3. The controller is modelled by using the fundamental block set of the XSG. For the designing of the integrator the Euler's forward method is considered. The equations presenting the discrete PI and 2 DoF control is presented in equation (5.2) and (5.3) respectively:

$$i_q^*(k) = i_q^*(k-1) + K_p(\omega_{er}(k) - \omega_{er}(k-1)) + K_i\omega_{er}(k-1)T_S \quad (5.2)$$

$$i_q^*(k) = i_q^*(k-1) + K_{p1}(\omega_{er}(k) - \omega_{er}(k-1)) + K_i\omega_{er}(k-1)T_S - K_{p2}(\omega_e(k) - \omega_e(k-1)) \quad (5.3)$$

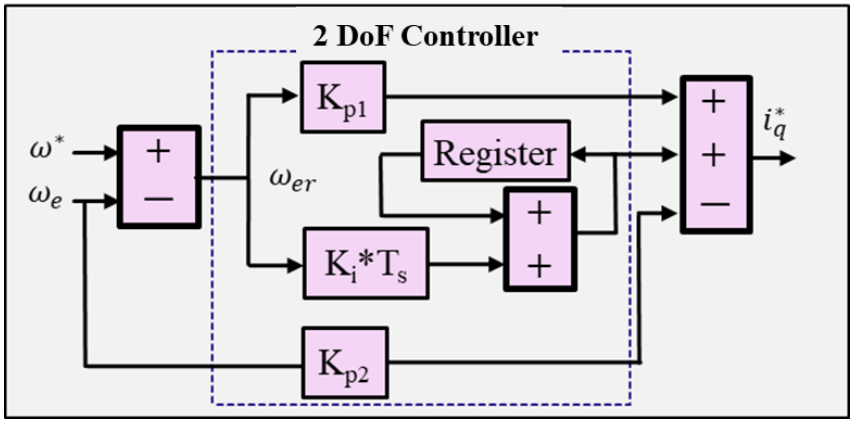


Fig.5.3 Digital implementation of 2 DoF PIP control

5.2.3 Average Switching Frequency

In case of the FS-MPC the switching frequency varies with respect to the sampling time. The switching frequency has a direct impact on the switching losses of the switching devices of the power converter. Moreover the system performance such as the total harmonic distortion (THD) and response time of the system are dependent upon the frequency at which the power device is operating. Therefore it is desirable to calculate the average switching frequency (f_{avg}) to have trade-off between the switching loss and also the system response. The average switching frequency per switching device can be calculated as follows:

$$f_{avg} = \Sigma \frac{S_{wa} + S_{wb} + S_{wc}}{T_{sw}} \tag{5.4}$$

Where f_{avg} is the average switching frequency. S_{wa}, S_{wb}, S_{wc} are the number of the switching cycles for the a,b,c phase switching devices and T_{sw} is the integral multiple of the fundamental frequency of the current.

5.3 Performance Validation

The performance of the controllers: 2-DoF PI and conventional PI for speed regulation with current control FS-MPC for the PMSM drive is investigated considering the system disturbances. The load disturbance, change in reference speed and harmonic distortion corresponding to sampling time is considered as following to demonstrate the controller performance.

5.3.1 Load Disturbance

The motor system is prone to the disturbances in the load and transient behavior of the system is considered in terms speed response corresponding to the load disturbance for system performance. A step change in load from low to high and high to low is included to demonstrate the performance under transient. The load is changed from 0.2 N-m to 1N-m at the instant of 0.52s and from 1 N-m to 0.6 N-m at the instant of 1s. The sampling time of 50μs is used for the FS-MPC. The speed response during transient demonstrated in Fig.5.4 for conventional PI and 2-DoF PI corresponding to reference speed.

The speed regulation performance of the 2-DoF PI control possessing reduced overshoot and undershoot for change in low load to high load and high load to low load condition correspondingly. Moreover, the settling for 2- DoF control has also improved and settling to the reference speed value faster as compared to that of the PI control.

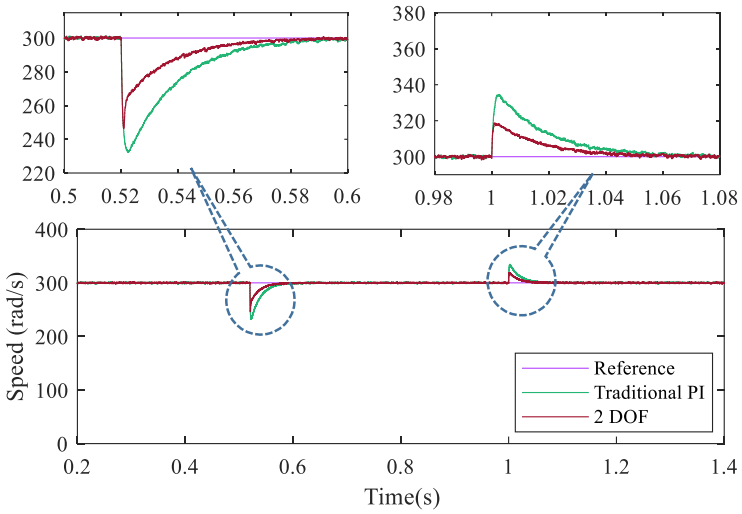


Fig.5.4. Motor speed response for PI and 2 DOF control with load disturbance

5.3.2 Speed Reference

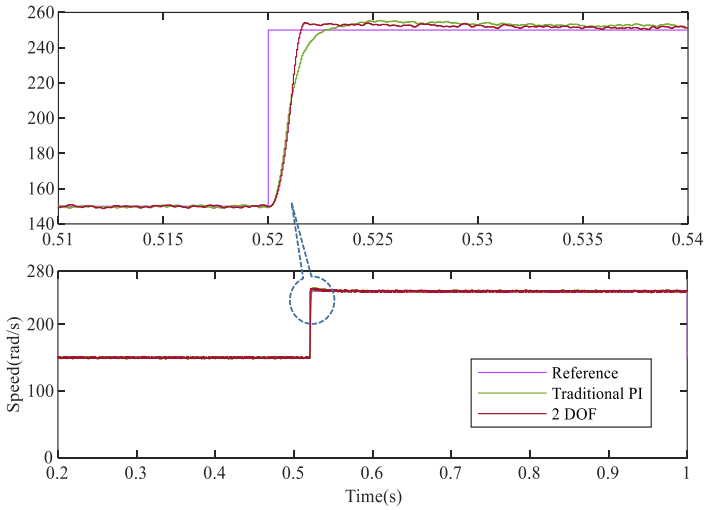


Fig.5.5. Motor speed response for PI and 2 DOF control with step change of the speed

The change in reference speed of the motor is also a considerable factor for different application. The motor may have to go through sudden change in speed and controller required to be responsive to regulate the speed corresponding to change in reference speed. A step change in reference speed of the motor from 150rad/s to 250rad/s at the instant of 0.52s is applied in Fig.5.5. To demonstrate the performance under transient condition of

speed response. The transient response of the 2-DoF control in terms of settling time is fast as compared to that of PI control.

5.3.3 Total Harmonic Distortion

TABLE 5.1 Comparison of THD

Sampling Time(μs)	PI		2DoF PI	
	f_{sw} (Hz)	THD%	f_{sw} (Hz)	THD%
100	758	11.85	708	11.50
50	1510	7.27	1429	6.32
40	1900	6.71	1850	5.18
30	2560	6.23	2522	4.18
20	3868	5.54	3826	4.11
10	7779	4.63	7739	4.64

TABLE 5.2 Comparison of the Controllers

		PI	2 DoF
f_{sw}		Slightly higher for all sampling time	Better for all sampling time
THD		Higher for all sampling time	Lower for all sampling time
Tuned parameter		2	3
Transient response	Settling time	Slow	Better
	Dynamic response	Higher	Better

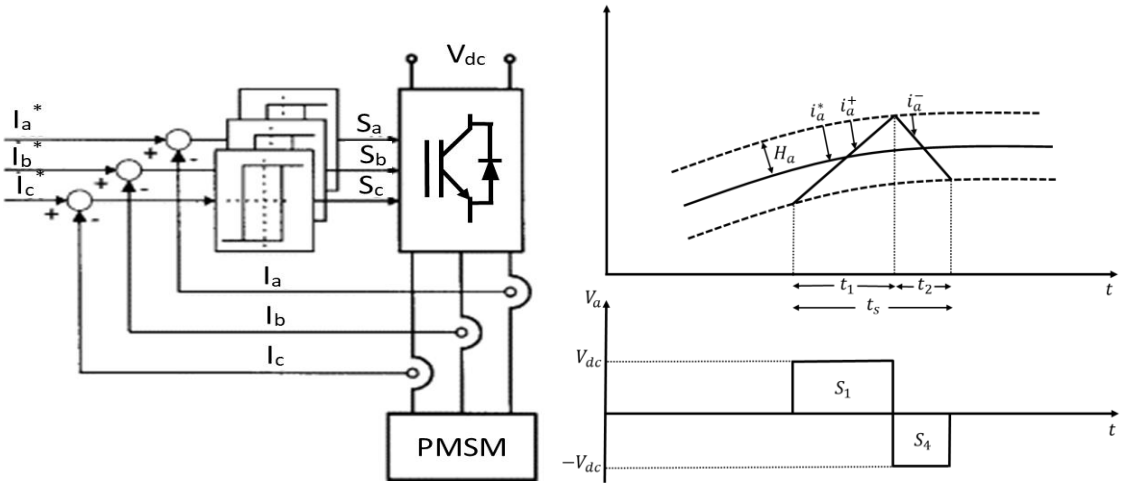
The performance of FS-MPC is governed by sampling time that ultimately impacts the harmonic distortion in three-phase currents. Therefore, the different sampling time is considered to investigate the performance of conventional PI and 2-DoF PI control. Table 5.1 illustrates the comparison of the THD and average switching frequency for both the controllers corresponding to different sampling time. In case of the 2-DoF speed control the average switching frequency is less as compared to that of the PI control. However, the THD in the three phase current in case of the 2-DoF control is also less compared to that

of the PI control. The comparative analysis of the performance for conventional PI and the 2-DoF control is summarized in Table 5.2.

5.4 FS-MPC for Constant Switching Frequency

5.4.1. Adaptive Band Calculations

The HCC is a nonlinear current control which generates the gate signals to the converter by passing the current error through the hysteresis band as shown in the Fig.5.6.a. The HCC using fixed hysteresis band for the PMSM drives results in variable switching frequency. To overcome this, a variable hysteresis band can be implemented for PMSM drive. For the hysteresis band an adaptive band has been adopted for making the switching frequency constant. For the calculation of the adaptive band the variation of the load and the neutral voltage of the motor is utilized. The neutral voltage is calculated by using the minimum voltage vector obtained by the MPC. The phase a current with hysteresis current control is shown in Fig.5.6.b.



(a) **(b)**

Fig.5.6. (a) General block diagram of the HCC (b) The current and voltage waveforms of phase 'a' for hysteresis current control.

The operation of the HCC depends upon the band and the current errors, when the current touches the lower band the upper switch of the inverter is on, while the current touches the upper band then the then lower switch of leg 'a' of inverter is switched on. The time interval t_1 and t_2 can be derived by following equations:

$$\frac{di_a^+}{dt} = \frac{1}{L_S}\left(V_{dc} - e_a - V_n\right) \tag{5.5}$$

$$\frac{di_a^-}{dt} = -\frac{1}{L_S}\left(V_{dc} - e_a - V_n\right) \tag{5.6}$$

L_s is the stator inductance, V_{dc} is the DC voltage, e_a is the back EMF voltage and V_n is the neutral voltage. i_a^+ and i_a^- are the rising and fall time currents. The neutral voltage of the motor is given by:

$$V_n = \frac{1}{3}\left(V_a + V_b + V_c\right) \tag{5.6}$$

From Fig.5.6b the following equations can be derived:

$$\frac{d}{dt}\left(i_a^+ - i_a^*\right) \times t_1 = 2H_a \tag{5.8}$$

$$\frac{d}{dt}\left(i_a^- - i_a^*\right) \times t_2 = -2H_a \tag{5.9}$$

$$t_1 + t_2 = T_S = \frac{1}{f_S} \tag{5.10}$$

Where t_1 and t_2 are the switching time interval for the upper switch and lower switch respectively and f_s is the switching frequency. Adding equation (5.8) and (5.9) gives

$$t_1 \frac{di_a^+}{dt} + t_2 \frac{di_a^-}{dt} - \left(t_1 + t_2\right)\frac{di_a^*}{dt} = 0 \tag{5.11}$$

Similarly subtracting equation (5.8) from (5.9), it gives

$$t_1 \frac{di_a^+}{dt} - t_2 \frac{di_a^-}{dt} - \left(t_1 - t_2\right) \frac{di_a^*}{dt} = 4H_a \tag{5.12}$$

Substituting the equations (5.5), (5.6), and (5.10) in equation (5.11) and (5.12) the following equations can be obtained.

$$t_2 - t_1 = -\frac{L_s}{V_{dc} f_s} \left[\frac{1}{L_s} \left(e_a + V_n\right) + \frac{di_a^*}{dt} \right] \tag{5.13}$$

$$t_2 - t_1 = \frac{4H_a - \frac{V_{dc}}{f_s L_s}}{\frac{e_a + V_n}{L_s} + \frac{di_a^*}{dt}} \tag{5.14}$$

From equation (5.14) and (5.10) the hysteresis band for phase ‘a’ is given by following expression

$$H_a = \frac{V_{dc}}{4 f_s L_s} \left[1 - \frac{L_s^2}{V_{dc}^2} \left\{ \frac{1}{L_s} \left(e_a + V_n\right) + \frac{di_a^*}{dt} \right\}^2 \right] \tag{5.15}$$

The counter EMF of the motor is given by:

$$e_a = -\omega_e \psi \sin \omega_e t \tag{5.16}$$

The adaptive band is depend upon the switching frequency, supply voltage back EMF, neutral voltage and slope of the command current wave. The slope of the command current wave can be changed to equivalent dc component for better implementation of the system. The phasor diagram of the motor is shown in the Fig.5.7.The d axis current was kept zero as mentioned above. At any instant of time the angle between the stationary reference frame axis and the magnetic axis is $\Theta_e = \omega_e t$.

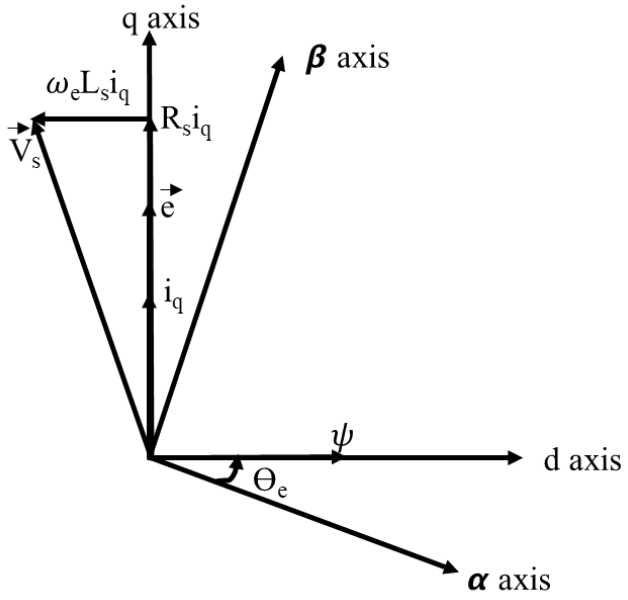


Fig.5.7. Phasor diagram of the PMSM motor.

From the Fig.5.7 the stator phase 'a' current can be written as:

$$i_a = -i_q sin\omega_e t \tag{5.17}$$

The differentiation of above equation gives:

$$\frac{di_a}{dt} = -\omega_e i_q cos\omega_e t \tag{5.18}$$

So the slope of the command current wave can be found by utilizing the above the equation (5.17).

$$\frac{di_a^*}{dt} = -\omega_e i_q cos\omega_e t \tag{5.19}$$

By substituting the equation (5.17) and (5.19) in (5.15) the hysteresis band for the phase 'a' is as follow:

$$H_a = \frac{V_{dc}}{4f_S L_S}\left[1 - \frac{L_S^2}{V_{dc}^2}\left\{\frac{1}{L_S}\left(-\omega_e f \sin\omega_e t + V_n\right) + -\omega_e i_q Cos\omega_e t\right\}^2\right] \quad (5.20)$$

Similar to the phase 'a' the hysteresis band for other phase are as same as it while with a phase displacement of $2\pi/3$. The neutral voltage can be evaluated by using the minimum voltage vector obtained by the FS-MPC. The switching frequency in equation (5.20) is depend upon the source voltage, band, rotor speed, reference current and the neutral voltage obtained from the switching pattern of the FS-MPC. Therefore by varying the hysteresis band the switching frequency of the inverter can be make constant.

5.4.2 MPC-DAHCC

To eliminate draw back of the variable switching frequency of FM-MPC, a combination of predictive control and adaptive hysteresis control is used. Moreover this technique has advantage of not using any modulator for generation of switching signals. The discrete adaptive HCC based FS-MPC for constant switching frequency is shown in the Fig.5.8.

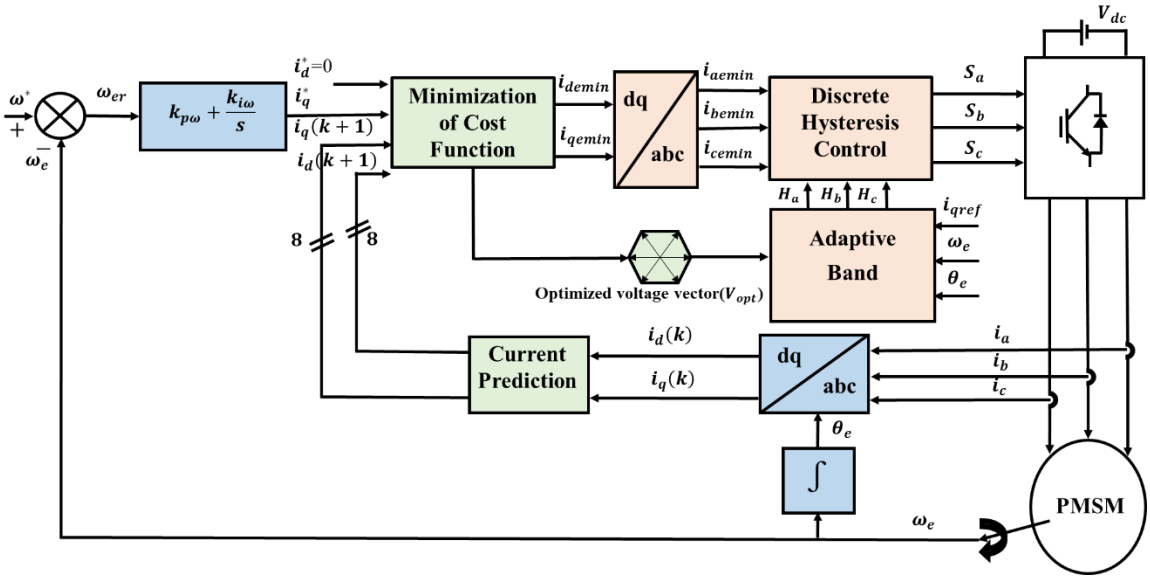


Fig.5.8 DHCC based FS-MPC

The optimized error obtained from the FS-MPC is passed through the adaptive hysteresis band to make the system work under constant switching frequency. The adaptive band from equation (5.20) is used for the hysteresis control. The adaptive band is depend upon the neutral voltage of the inverter. This neutral voltage can be obtained from the optimized voltage vector for the minimization of the cost function. The steps for the proposed current controller is given bellow:

- Generation of the reference current signal: iq^* by using the speed control loop and id^* kept zero.
- The three phase PMSM current $i(k)$ at the present sampling instant k is measured and converted to dq axis by using Clarke transform. Then the dq axis measured current is given to current prediction for the prediction of the future variables.
- The PMSM current for the sampling interval $(k+1)$ is predicted corresponding to the possible switching states of the inverter.
- The cost function G, as per equation (8) is calculated using the predicted load current $i\ (k+1)$ and reference current $i^*\ (k)$.

5.5 System Implementation

The system considered for the implementation consists of three phase voltage source inverter, three phase PMSM and the control. The power circuit (three phase VSI, Motor) is designed in the MATLAB/Simulink and the control part is implemented by using the fundamental blocks of XSG which is integrated to the MATLAB/Simulink. The controller algorithm then verified through HIL simulation. The schematic diagram representing the system implementation is shown in Fig.5.9. The steps for the implementation of the PMSM drive is explained in two sections.

5.5.1 FS-MPC

The predictive model of the motor drive system consist of three steps. Prediction of the motor current, evaluation of cost function and finally generation of switching signal corresponding to the minimization of the cost function. For the digital implementation of

FS-MPC the Xilinx block set are used for the modeling. A model based approach has been adopted (similar to chapter 4) for the implementation of the FS-MPC in XSG for HIL

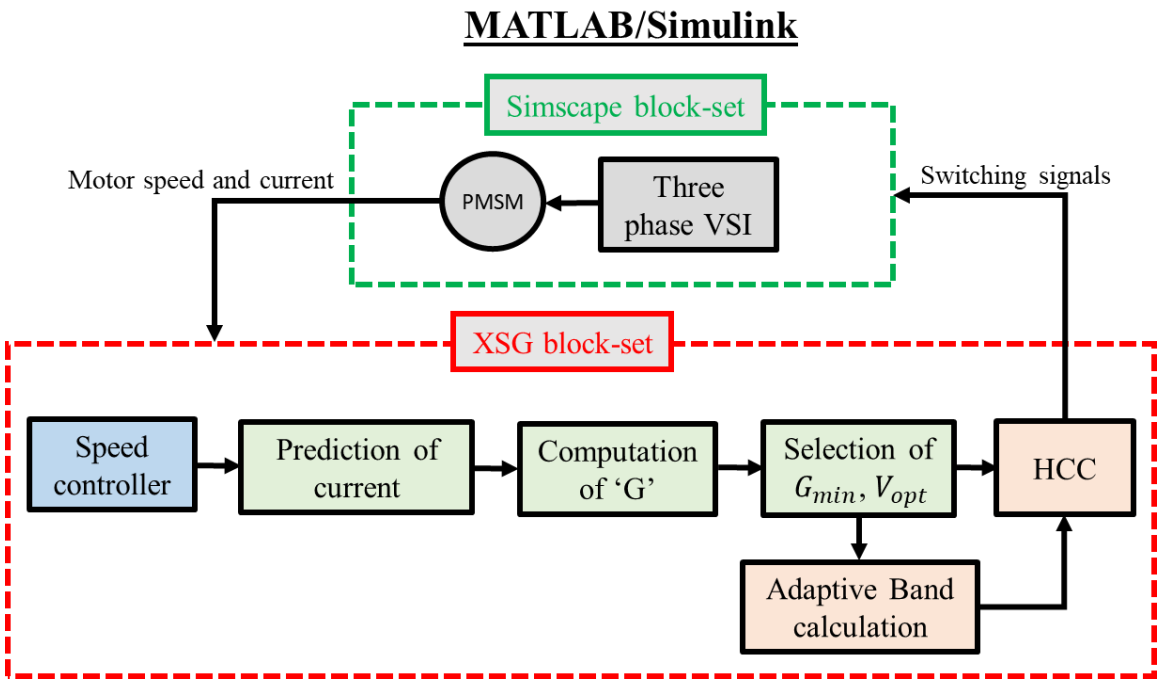


Fig.5.9. System implementation

5.5.2 Modelling of the Adaptive HCC

The switching signal generation for the phase 'a' by adaptive based HCC is demonstrated in Fig.5.10. The adaptive HCC generate switching signal by passing the current error I_{aemin} through adaptive band H_a. The adaptive band given in equation (5.20) is modeled by using the fundamental block set of the XSG for HIL Simulation. The implementation of the HCC is done by using the comparator and the SR-flip flops. The optimized current error which is obtained by the FS-MPC is compared with the variable hysteresis band. Finally the output of the comparator is fed to the flip flop for generation of the switching signal.

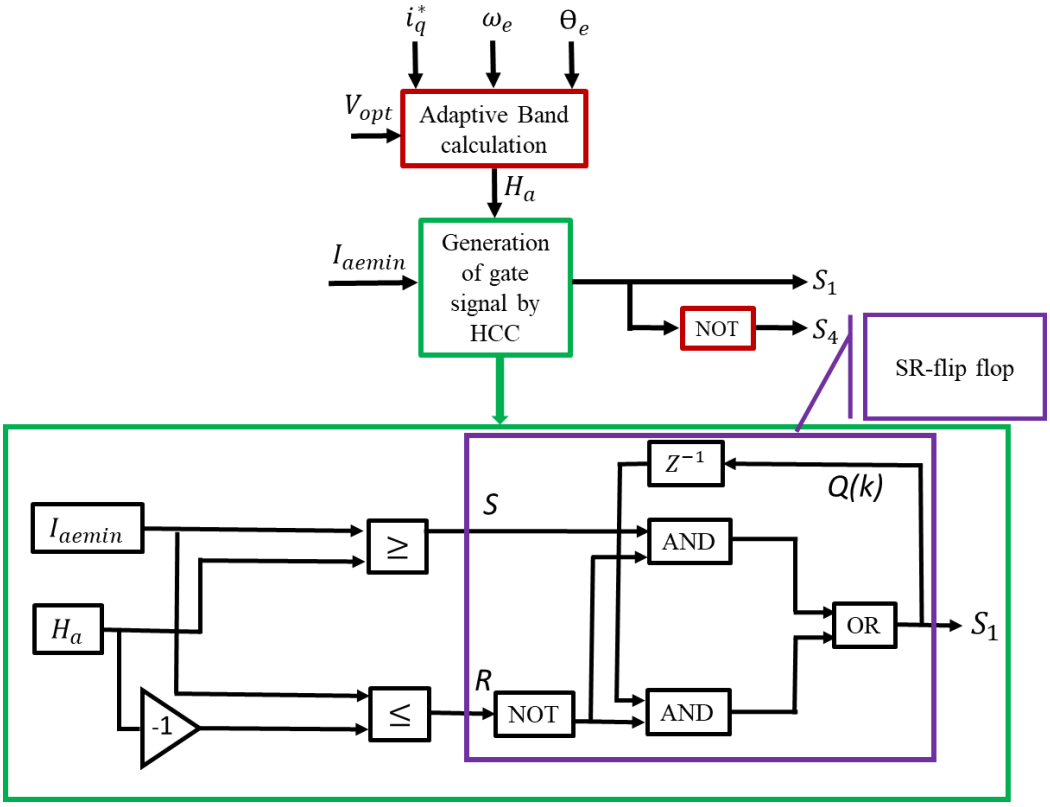


Fig. 5.10 Implementation of DAHCC

To implement the SR-flip flop in the Xilinx system generator the Boolean expression from the truth table of the SR-flip flop is utilized. The Boolean expression of the SR-flip flop is given by:

$$Q(k+1) = \bar{R}S + \bar{R}Q(k) \tag{5.21}$$

The output of the flip flop *Q(k)* is feedback by using the memory block in the XSG block set.

5.6 Performance Validation

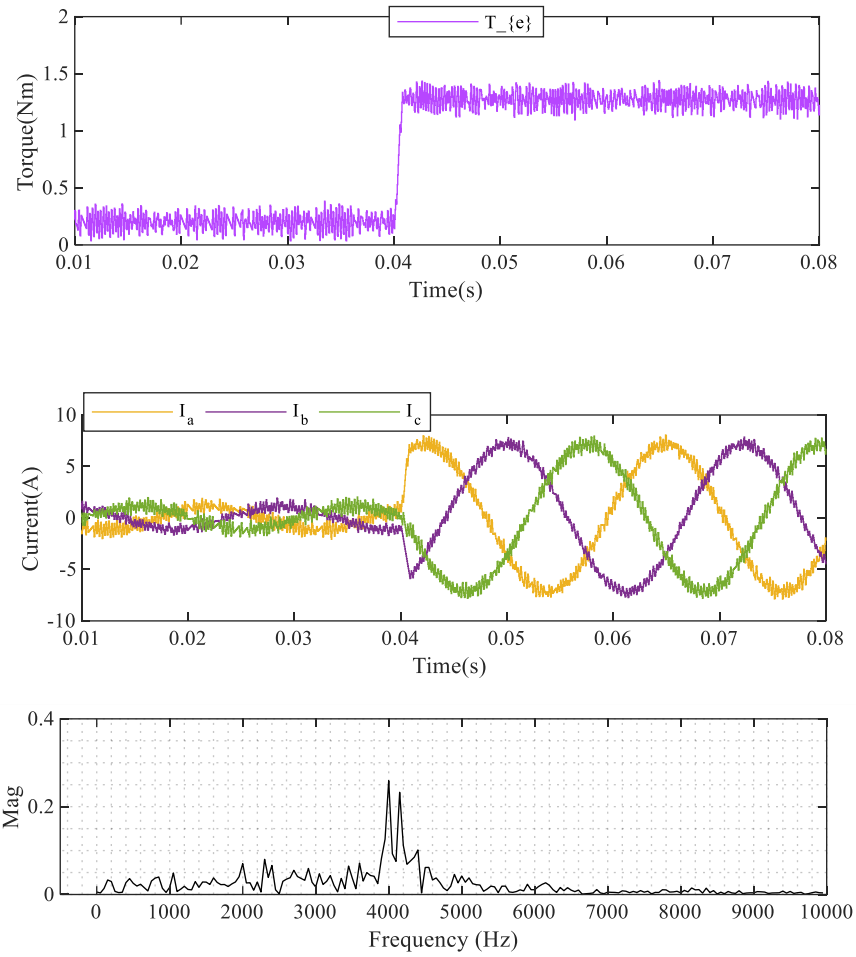
The performance of the VSI fed PMSM drive system is compared for the proposed FS-MPC with constant switching frequency and conventional FS-MPC and to the HCC with constant switching frequency. The stator current performance and speed performance

with change of load torque is considered for the analysis of the proposed MPC-DAHCC. Moreover a detail analysis of dynamic current response and speed response of the system is also presented.

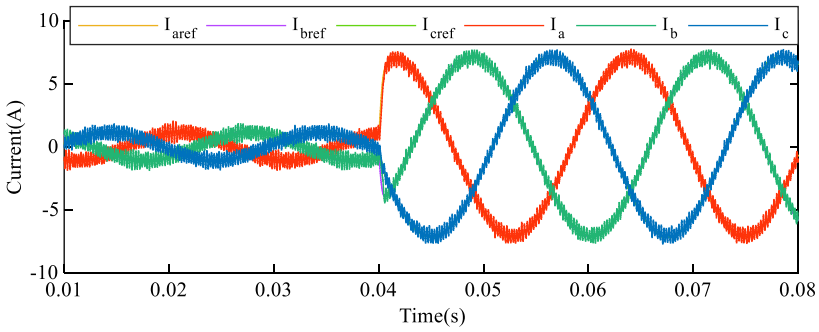
5.6.1 System Behavior

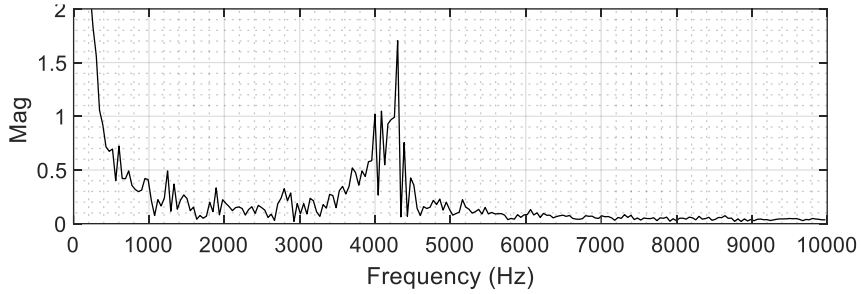
The change in motor load condition is considered to validate the controller performance during the transient condition. For the case of FS-MPC, the load torque and three phase current of the motor is demonstrated in Fig. 5.11 (a) under transient condition. The load torque is changed at the instant of 0.04s from initial condition of 0.2N-m to the rated condition of 1.27 N-m. The frequency spectrum of motor current corresponding to the rated load condition is also illustrated in the Fig.5.11 (a).The variable switching frequency leads to the frequency spectrum spread from zero to seven kHz.

The motor three phase current is for the HCC and HCC with constant switching frequency is illustrated in the Fig.11. (b) and (c). The predefined frequency is chosen to be 5 kHz. The frequency spectrum of the motor current is concentrated around 5 kHz. Similarly the three phase current of motor is demonstrated in the Fig.5.11 (d) for the MPC-DAHCC. To demonstrate the effectiveness of the controller regarding constant switching frequency, the frequency spectrum of the motor current is demonstrated in Fig.5.11 (d). The frequency spectrum of the proposed one is almost concentrated around the predefined switching frequency of five kHz that authenticates the operation of motor under constant switching frequency. The switching frequency of the MPC-DAHCC is operate exactly at the predefined switching frequency however the HCC with constant switching frequency is operate at lower switching frequency. Therefore by comparing all the technique the MPC-DAHCC gives a better response.

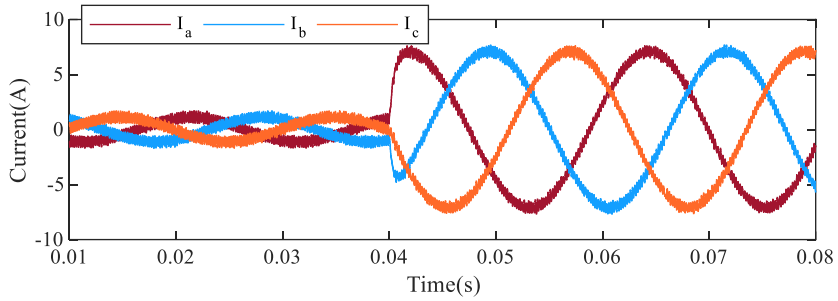

T_{e}
Torque(Nm)
Time(s)
I_a
I_b
I_c
Current(A)
Time(s)
Mag
Frequency (Hz)

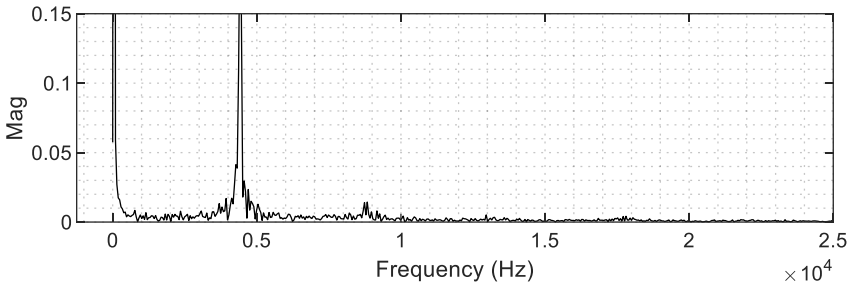
(a)


I_aref
I_bref
I_cref
I_a
I_b
I_c
Current(A)
Time(s)

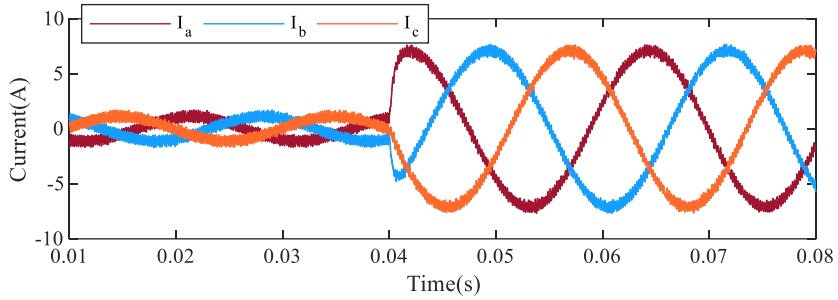

Mag
Frequency (Hz)

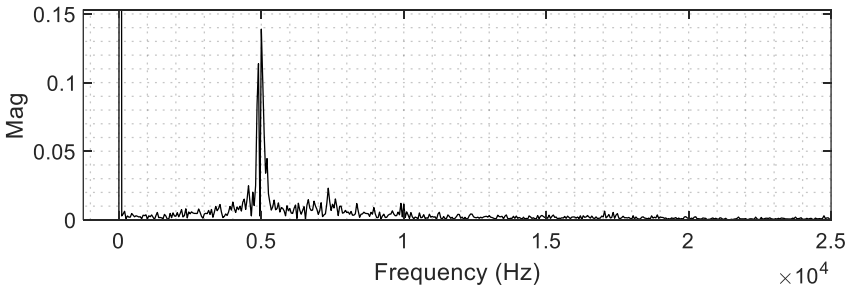
(b)


I_a
I_b
I_c
Current(A)
Time(s)


Mag
Frequency (Hz)
×10^4

(c)


I_a
I_b
I_c
Current(A)
Time(s)



(d)

Fig.5.11. Electromagnetic torque, three phase current and Frequency Spectrum (a) for FS-MPC (b)HCC (c) HCC with constant switching frequency for MPC-DHCC with T_s=10 µs.

5.6.2 Intermediate Response

The adaptive three phase hysteresis band for the MPC-DAHCC is shown in the Fig.5.12. The adaptive band is obtained corresponding to the constant switching frequency of 5 kHz. The width of the adaptive band changes with change of load at the instant *T=0.04s*.

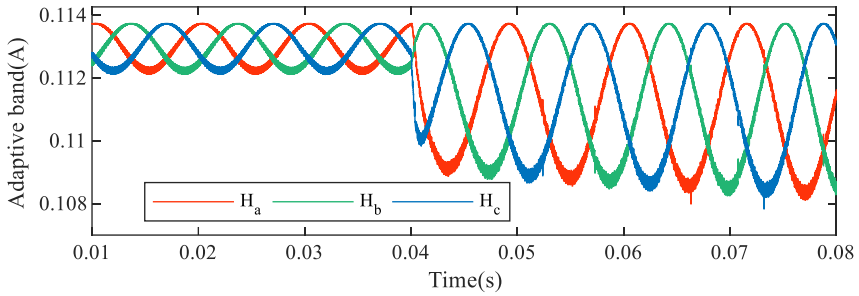
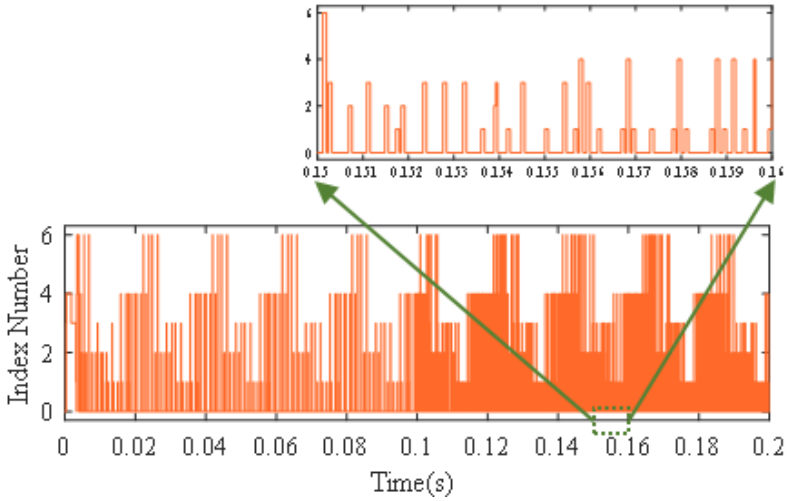
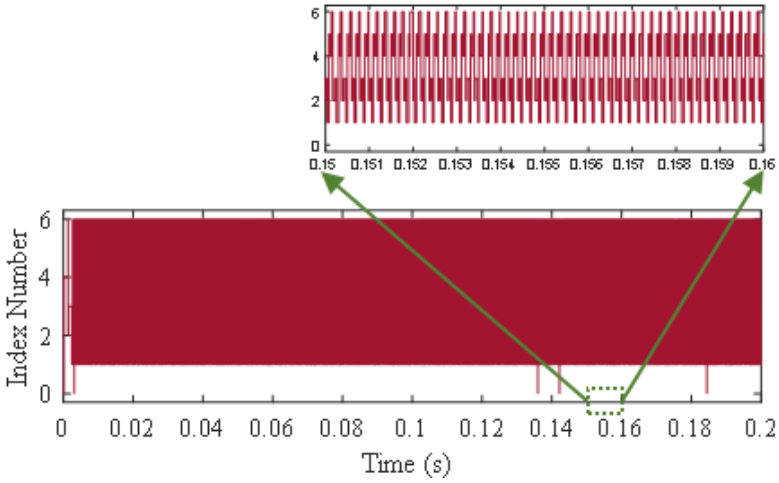


Fig.5.12. Three phase adaptive band for the MPC-DHCC

The index number selection for both the FS-MPC and the MPC-DHCC is shown in the Fig.5.13. For the FS-MPC the optimal switching vector are selected corresponding to the index number. Whereas the index number of the MPC-DAHCC is used for the evaluation of the neutral voltage of the system. The index number of MPC-DAHCC follows a particular pattern for the entire duration of time. However for conventional FS-MPC, it follow a random pattern. Therefore, the Switches are not commuted at fixed sampling time which make the control to work in the variable switching frequency. However for a particular pattern of the MPC-DAHCC works at predefined switching frequency.



(a)



(b)

Fig.5.13. Index number for the a. FS-MPC b. MPC-HCC

5.6.3 Total Harmonic Distortion

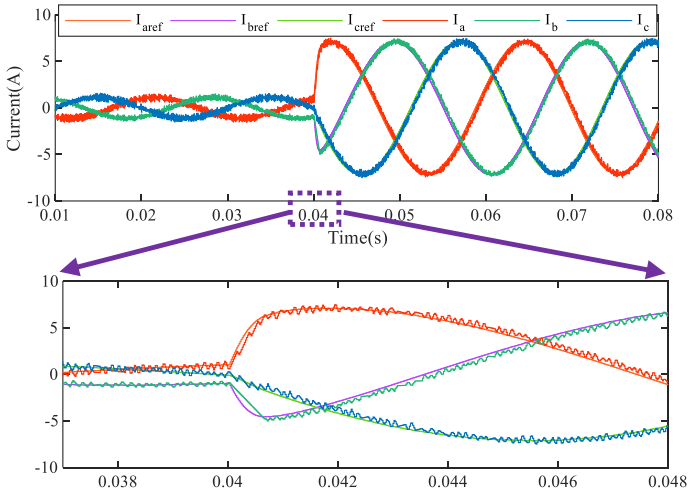
Table 5.3 gives comparison of the THD for both the cases at different sampling time. In case of the FS-MPC switching frequency depend upon the sampling frequency. The maximum switching frequency of the FS-MPC is half of the sampling frequency. For conventional FS-MPC shows low THD at high sampling frequency. However the maximum switching frequency and the average switching frequency increases with the

increase in the sampling frequency. In case of MPC-DAHCC the THD decreases with increase of the sampling frequency. Moreover the switching frequency remain constant. At same sampling time the MPC-DHCC has lower THD as compared to that of the FS-MPC and also the average switching frequency of the FS-MPC is more than that of the MPC-DAHCC.

Table 5.3 THD Comparison

Control	Case	Sampling time(µs)	Switching frequency (KHz)	Average switching frequency (KHZ)	THD (%)
FS-MPC	1	50	Max-10	2.820	10.24
	2	40	Max-12.5	3.573	9.80
	3	30	Max-16.6	4.837	8.52
	4	20	Max-25	7.413	7.71
MPC-DHACC	5	20	5	4.853	7.22
	6	10	5	4.979	5.17
	7	5	5	5.031	4.8

5.6.4 Dynamic Response



(a)

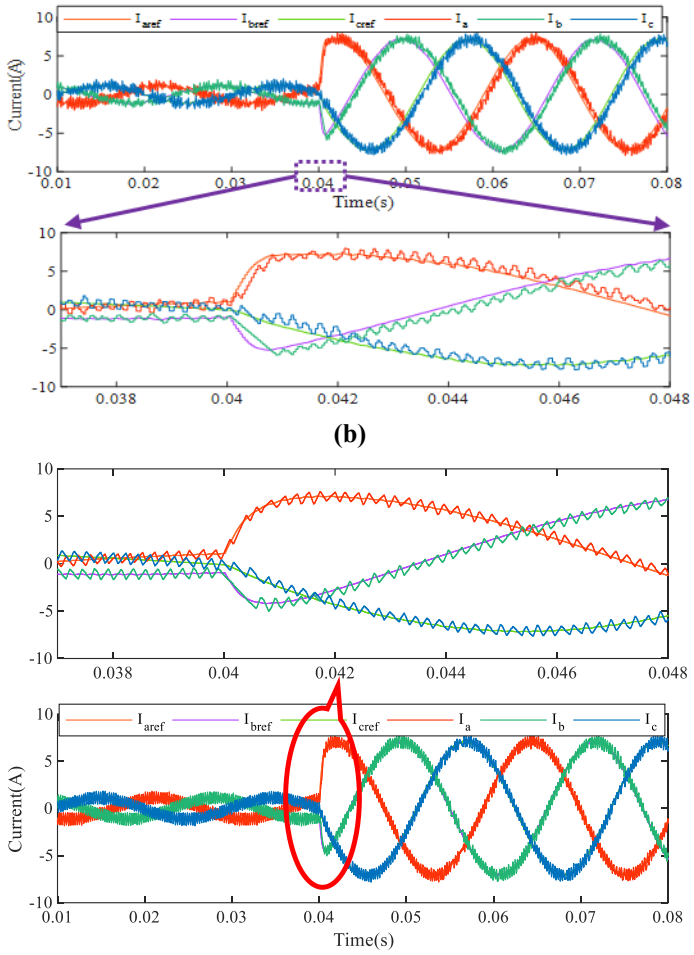


Fig.5.14. The current tracking performance (a) FS-MPC for T_s=20μs (b) FS-MPC for T_s=40μs (c) MPC-DHCC for T_s=20μs

To investigate the dynamic response of the system the current response and the speed response are considered for a load change of 0.2 Nm to 1.27Nm at the instant T=0.04s.The tracking performance i_a, i_b and i_c corresponding to the i_{aref}, i_{bref} and i_{cref} for T_s=20 μs and 40 μs is demonstrated in Fig.14 (a) and (b) and For MPC-DAHCC for T_s=20 μs is demonstrated in Fig.14 (c). The tracking performance for the FS-MPC case shows a delay response.

The current tracking performance for the FS-MPC corresponding to T_s=20 μs is better compared to T_s=40 μs. The current tracking performance improved corresponding to the increase in sampling frequency. However that will lead to the wider frequency

spectrum due to increase in maximum switching frequency. The current tracking performance of the MPC-DAHCC corresponding T_s=20 µs is better as compared to the FS-MPC for both the sampling time T_s=20 µs and T_s=40 µs.

In addition, the motor speed response for both the FS-MPC and the MPC-DAHCC is demonstrated in the Fig.5.15. There is a droop in the speed response for the FS-MPC as compared to the MPC-DAHCC.

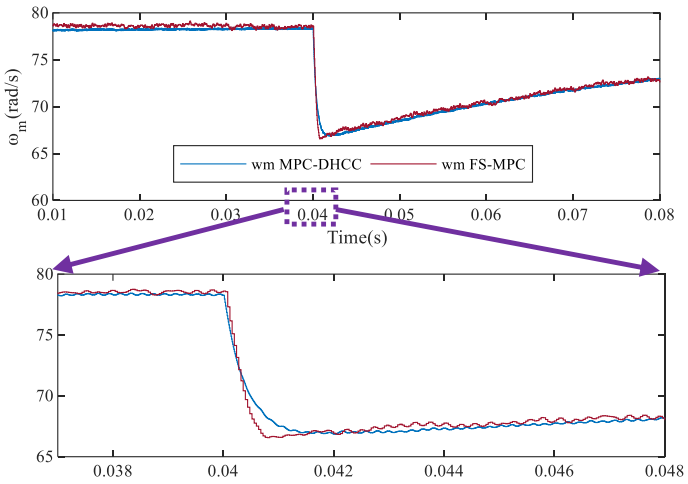


Fig. 5.15. The motor speed response for both FS-MPC and MPC-DHCC for T_s=20µs.

5.7 Summery

The dynamic response of FS-MPC is one of the major factors that stands out amongst the controller family. Nevertheless, the motor speed regulation required additional control and generally a conventional proportional-integral (PI) controller is used. In this chapter the 2 DOF speed control based FS-MPC is implemented for the regulation of the speed of the PMSM drive system. The proposed control is validated by comparing it with the conventional PI control. The controller illustrates a better dynamic performance as compared to that of the conventional PI control considering both change in the load disturbance and change in the speed reference. The 2-DoF PI control presented in the chapter is capable of achieving faster dynamics as compared to its counterpart. Moreover, it has demonstrated the better performance in companionship of PI based FS-MPC

considering switching frequency is reduced corresponding to cases of different sampling time.

In addition to the faster dynamic response the FS-MPC exploits the advantages such as high flexibility. However, the spread spectrum due to variable switching frequency of FS-MPC is the main drawback associated with it. This Chapter presents an adaptive HCC based FS-MPC for the VSI fed PMSM drive system which allows the system to work at predefined switching frequency. FS-MPC have inherently discrete nature and discrete adaptive HCC is designed for system implementation. In order to validate the system performance it compared with the FS-MPC, HCC, and HCC with constant switching frequency. The analysis is done by considering the switching frequency behavior and dynamic performance. The control shows a better performance in terms of the THD with advantage of constant switching frequency. Moreover it gives a better dynamic performance as compared to the other controller.

Moreover a model based approach has been adopted for the system implementation as in chapter 4 for modeling of FS-MPC and DAHCC. The simulation of the system has been done using the Xilinx system generator (XSG) and MATLAB/Simulink simulation environment for the HIL simulation.

Chapter 6

CONCLUSIONS AND FUTURE WORK

6.1 Conclusions

The various conventional, as well as modern control schemes, have been used motor drive system, for the specific control objectives. The control schemes have to deal with various pros and cons, however, every control scheme has its distinctive characteristics that make the particular control scheme more suitable for a specific application.

The first procedure is to implement the conventional control (FOC) PMSM drive system. In general, the sampling rate of the speed controller is slower as compared to that of the sampling rate of the current controller. As the control loops operate at different data sampling rate, the impact of time synchronization between these controllers is a crucial concern considering the transient conditions corresponding to the sampling rates. In chapter 3, an FPGA based design and development of PMSM drive system considering the impact of time-synchronization for feedback control loop corresponding to sampling frequencies is presented. A step by step and case by case time synchronizations methodology is considered to analyze the repercussion of sampling frequencies corresponding to feedback control loop synchronization. This controller has to tune at least six parameter and also has a sluggish behaviour of motor drive system.

The modern control can be alternative solution to overcome this issue. The FS-MPC as a modern control is one of the categories of a wide family of the MPC that has been utilized for the power converters and drives due to its appealing characteristics especially the one to handle multiple control variables simultaneously. However, FS-MPC has to deal with some issues such as computational delay during real-time implementation, a variable switching frequency, high switching frequency requirements for enhanced

performance, an issue of model parameter mismatch and a non-zero steady-state error. In this work, different approaches were proposed to tackle some issues of the FS-MPC.

The implementation of FS-MPC algorithm use two major computation steps: the predictive model and the cost function were formulated considering the motor current control objective of the three-phase two-level VSI system. However, the cost function optimization problem is computed by a predicting all the possible switching states of the power converter in every sampling period. When the complexity in the converter system increases the system may undergo delay which ultimately degrade the system performance.

To overcome the computational delay issue of the FS-MPC, the controller was implemented using an FPGA through the controller development on a model based design platform of a Xilinx digital simulator (XSG) as discussed in chapter 4. The XSG platform facilitates an automatic HDL code generation for the straightforward implementation of the system using FPGA. The MBD platform is considered advantageous for rapid controller development and prototyping using easy debugging. The XSG platform facilitates the HIL simulation environment that is an intermediate stage between the software simulation and the actual experimental system implementation.

To validate the performance in a real-time environment, the XSG modelling of the FS-MPC was utilized to generate the HDL code automatically for the FPGA-based system implementation. The conventional control and modern control for PMSM drive was considered for the physical system implementation. A comparative analysis between the conventional control and FS-MPC was presented through the experimental results considering the performance indices of dynamic response and total harmonic distortion. Fast dynamic response of the FS-MPC was validated through experiment by motor speed tracking with step changes in the reference and load disturbance as well. The FS-MPC give better performance in terms of transient response.

The dynamic response of FS-MPC is one of the major factors that stands out amongst the controller family. Nevertheless, the motor speed regulation required additional control and generally a conventional proportional-integral (PI) controller is used. In chapter 5, a 2-DoF control strategy is considered to enhance the dynamic performance of motor speed

regulation. The 2-DoF control design is consisting of a conventional PI controller and an additional proportional gain as a feedforward loop. The 2-DoF control along with FS-MPC is employed for the PMSM drive system. The 2-DoF PI control presented is capable of achieving faster dynamics as compared to its counterpart. Moreover, it has demonstrated the better performance in companionship of PI based FS-MPC considering switching frequency is reduced corresponding to cases of different sampling time.

The main drawback with this technique is variable switching frequency which ultimately leads to increase in switching losses, spread switching frequency spectrum and poor system performances. The switching harmonic spectrum depends on the commutations of the converter's power switches, which in FS-MPC is not guaranteed to occur at the fixed sampling frequency. Due to the variable switching frequency the filter design and the thermal design became more difficult which leads to the increase of the overall cost of the system. In this work, a predictive control strategy with fixed switching frequency is proposed. A discrete adaptive based hysteresis current control (DAHCC) is combined with the basic FS-MPC as current controller to achieve constant switching frequency. The controller is validated through HIL simulation. The controller can achieve constant switching frequency with better dynamic performance considering different sampling frequency.

6.2 Future Scope of Work

The possible future scope of work using the control scheme FS-MPC is mentioned here.

1. The hybrid controller MPC-DAHCC, 2 DOF based MPC has implemented through the HIL simulation. The controllers can be implemented through real time FPGA for its validation.
2. The controller depends upon the system parameter. To compensate for the effect of model parameter mismatch in the physical system implementation, an adaptive based predictive model can be used that can automatically update the system parameter.
3. The control scheme was implemented using an FPGA through the controller development in a digital platform of XSG for the PMSM drive. This approach can pave the path for designing realistic and efficient controllers in Power Electronic converter applications.

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